Università degli studi Roma Tre

Scuola Dottorale in Scienze Matematiche e Fisiche

Sezione di Fisica - XXII ciclo

Design, construction and tests of a high resolution, high dynamic range Time to Digital Converter

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Pensiero del giorno per Salvatore:

"la vera grandezza è basata non sulla potenza e l'orgoglio culturale, ma sulla vera sapienza la quale fa discernere i veri valori e si trasforma in sorgente di vita.....

Per essere sapienti occorre anche studiare un po'. Coraggio!"

Babbo.

Quanto poi alla misura del tempo,
si teneva una gran secchia piena d'acqua,
attaccata in alto, la quale per un sottil cannellino,
saldatogli nel fondo, versava un sottil filo d'acqua,
che s'andava ricevendo con un piccol bicchiero
per tutto 'l tempo che la palla scendeva nel canale e nelle sue parti:
le particelle poi dell'acqua, in tal guisa raccolte,
s'andavano di volta in volta con esattissima bilancia pesando,
dandoci le differenze e proporzioni de i pesi loro
le differenze e proporzioni de i tempi;
e questo con tal giustezza, che,
come ho detto, tali operazioni,
molte e molte volte replicate,
già mai non differivano d'un notabil momento.

Estratto da *"Discorsi e dimostrazioni matematiche intorno a due nuove scienze"* di *Galileo Galilei.*

Contents

Introduction

The needs of future High Energy Physics (HEP) experiments require the use of time measurements systems with remarkable benefits in terms of resolution, dynamic range and high operating frequency.

This thesis is focused on the development and evaluation of high resolution and long range Time to Digital Converter (TDC) architectures suitable for the measurement of ~100 ns time intervals, ~100 ps resolution and MHz repetition rate in the context of the detectors of the KLOE experiment.

The KLOE experiment has been designed in order to record e^+e^- collisions at DAΦNE, the ϕ-factory at the Laboratori Nazionali di Frascati.

DAΦNE collider operates at high luminosity at the center of mass energy corresponding to the mass of the ϕ resonance, 1020 MeV. The ϕ-meson decays mostly to kaon pairs. The ϕ production cross section peaks at about 3 μbarns. Many interesting physics measurements can be performed with the luminosity reached by DAΦNE (5×10^{32} cm^{-2} s^{-1}); more than thousand ϕ-mesons are produced per second. The rate of $e^+e^- \rightarrow e^+e^-$ elastic scattering and $e^+e^- \rightarrow e^+e^-$ X via $\gamma\gamma$ interaction is much higher. The trigger and data acquisition systems of the KLOE experiment allow for a repetition rate of about 20 kHz.

The thesis work is aimed to the specific requirements of the HEP experimental environment; nevertheless, it is also useful in many applications of science and industry where high resolution time measurements are required.

The structure of this thesis is organized as follows.

In the first chapter, the DAΦNE collider and the KLOE experiment are described. A brief description of the physics goals of the experiment and the systems needed to achieve it are given.

In the second chapter a review of methods for time interval measurements is given; the basic and most important parameters of a TDC are described.

The third chapter is dedicated to the two TDC architectures implemented in a Field Programmable Gate Array (FPGA) device.

The fourth chapter describes the TDC tester board, that I built in order to test the TDC architectures, and the test environment.

In the fifth chapter, I compare the two architectures and show their performance in terms of stability and resolution.

Chapter six is dedicated to the summary of the test results.

Chapter 1

Physics with KLOE

1.1 Introduction

The scientific program with a high-performance detector such as KLOE (K-Long Experiment) covers several fields in particle physics: from measurements of interest for the development of the Effective Field Theory (EFT) in quark-confinement regime to fundamental tests of Quantum Mechanics (QM) and of discrete symmetries, CP and CPT invariance. It includes precision measurements to probe lepton universality, the Cabibbo-Kobayshi-Maskawa (CKM) unitarity and settle the hadronic vacuum polarization contribution to the anomalous magnetic moment of the muon and to the fine-structure constant at the M_Z scale.

During year 2008 the Accelerator Division of the Frascati Laboratory has tested a new interaction scheme on the DAΦNE (Double Annular ϕ-factory for Nice Experiment) ϕ-factory collider, with the goal of reaching a peak luminosity of 5×10^{32} cm^{-2} s^{-1}, a factor of three larger then what previously obtained. The test has been successful and presently DAΦNE is delivering up to 15 pb^{-1}/day, with solid hopes to reach soon 20 pb^{-1}/day [1,2]. Following these achievements, the data-taking campaign of the KLOE detector on the improved machine that was proposed in 2006 [3], will start in 2010.

1.2 DAΦNE

The DAΦNE layout is shown in figure 1.1. The collider is made of two storage “rings” in which 120 bunches of electrons and positrons are stored. Each bunch collides with its counterpart once per turn. The two separate rings scheme is intended to minimize the perturbation of each beam on the other. Electrons and positrons are injected in the rings in bunches separated by 2.715 ns at the energy of ~510 MeV, and collide at an angle of (π – 0.025) radians. Electrons are accelerated to the final energy in the Linac (Linear Accelerator), accumulated and cooled in the accumulator ring and injected in the electron ring with a transfer line.

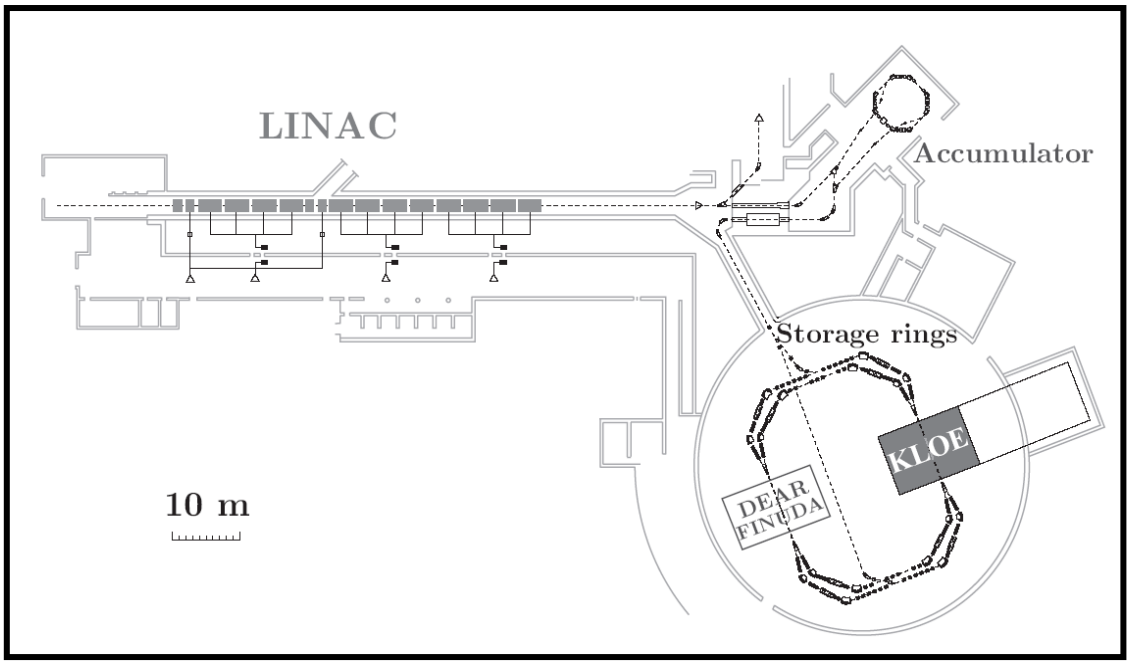


Figure 1.1: The DAΦNE complex.

Positrons require first electrons accelerated to 250 MeV to an intermediate station in the Linac, where positrons are created in a thin target, then follow the same processing as electrons and are injected with another transfer line. Since the stored beam intensities decay rapidly in time, the cycle is repeated three-four times per hour. The luminosity is defined by the beam parameters:

$$L = n\frac{\nu N^{+}N^{-}}{4\pi\sigma_x\sigma_y} \qquad (1.1)$$

where *n* is the number of the bunches, each collecting N particles, ν is the revolution frequency in the storage ring (367 MHz), σ_x and σ_y are the standard deviations of the horizontal and vertical transverse beam profile at the interaction point.

DAΦNE runs mostly at a center-of-mass energy of $M_\phi \approx 1019.45$ MeV. The ϕ production cross section is $\sigma(e^+e^- \rightarrow \phi) \approx 3.1$ μb. The dominant ϕ meson decays [4] are shown in table 1.1.

Decay mode	Branching ratio
K^+K^-	$(48.9 \pm 0.5)\%$
$K^0_L K^0_S$	$(34.2 \pm 0.4)\%$
$\rho\pi + \pi^+\pi^-\pi^0$	$(15.32 \pm 0.32)\%$
$\eta\gamma$	$(1.309 \pm 0.024)\%$
$\pi^0\gamma$	$(1.27 \pm 0.06)\times 10^{-3}$
e^+e^-	$(2.954 \pm 0.030)\times 10^{-4}$
$\mu^+\mu^-$	$(2.87 \pm 0.19)\times 10^{-4}$
$\eta\, e^+e^-$	$(1.15 \pm 0.10)\times 10^{-4}$

Table 1.1: Main branching ratios of ϕ meson decays .

1.3 KLOE

KLOE is a multipurpose detector, mainly consisting of a large cylindrical Drift Chamber (DC) with an internal radius of 25 cm and an external radius of 2 m, surrounded by a sampling fibers calorimeter (EMC) organized in a barrel and two end-caps. Both DC and EMC are immersed in the 0.52 T axial magnetic field of a superconducting solenoid.

The design was driven by the intent of being a definitive high precision experiment, while the size was dictated by the long decay length of the K_L meson. Kaons from ϕ mesons decaying at rest travel at approximately one fifth of the speed of the light; the mean path travelled by a K_L meson $\lambda_L = \beta\gamma c\tau$ is 3.4 m; with a radius of about two meters, KLOE can catch ~50% of K_L decays.

Peculiar to KLOE is the spherical, 10 cm radius, beam pipe which allows all of the K^0_S mesons produced in ϕ meson decays to move in vacuum before decaying (λ_S is 6 mm). Details of the detector can be found in refs. [5-9]. A transverse view of the KLOE detector is shown in figure 1.2.

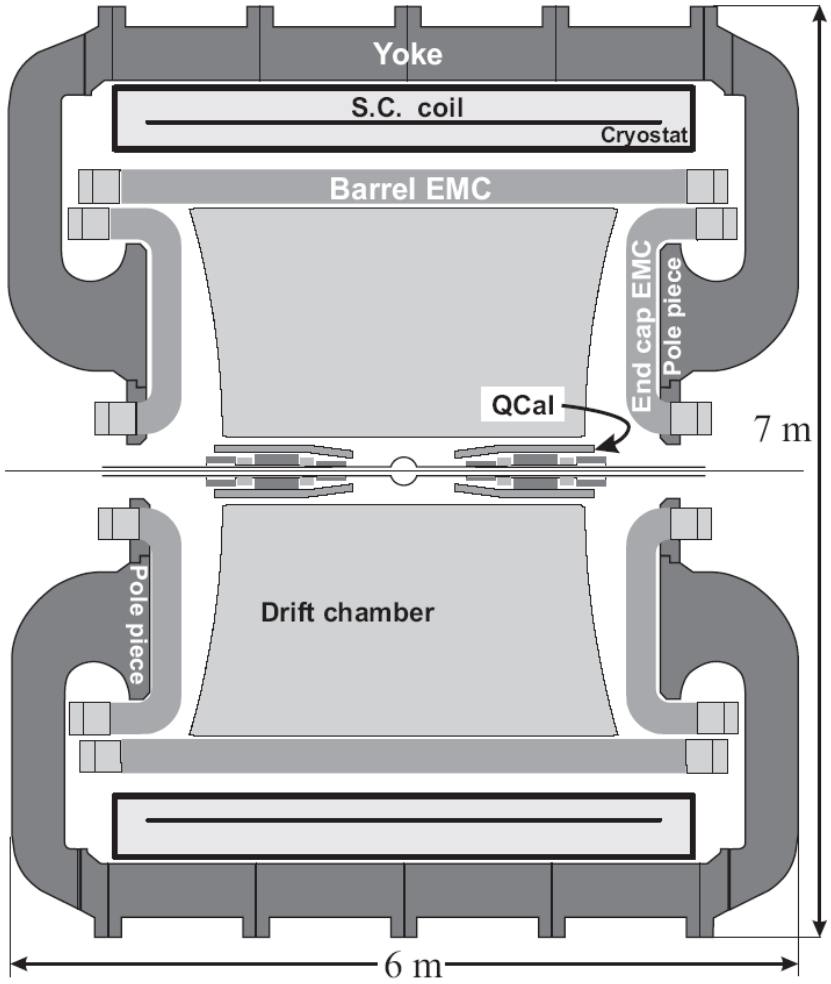


Figure 1.2: Cross-sectional view of the KLOE experiment, showing the interaction region, the DC, the EMC, the superconducting coil, and the return yoke of the magnet, the beam pipe with the spherical insertion, the low-β quadrupoles for the beam final focus and the two QCAL calorimeters around them.

From 2000 to 2006, KLOE has acquired 2.5 fb^{-1} of data at the $\phi(1020)$ peak, plus additional 250 fb^{-1} at energies slightly higher or lower. A collection of the main physics results of KLOE can be found in Ref. [10].

1.4 KLOE-2

For the forthcoming DAΦNE run [11], upgrades have also been proposed for the detector; the entire plan of the run is referred as the KLOE-2 project [12]. In a first phase, two different devices named Low Energy Tagger (LET) and High Energy Tagger (HET) will be installed along the beam line to detect the forward scattered electrons/positrons from $\gamma\gamma$ interactions. Two LET detectors will be installed at about 1 meter away from the interaction point (inside KLOE); while two HET detectors will be installed at about 11 meters away from the interaction point, just after the first bending magnets. The positions for these tagging detectors were chosen on the basis of the DAΦNE magnetic elements, used as a beam spectrometer, and the available free space along the beam lines. The two e^+e^- energy ranges they explore are: 160-230 MeV for the LET and 425-490 MeV for the HET. Figure 1.3 shows the positions of the detectors along the beam line.

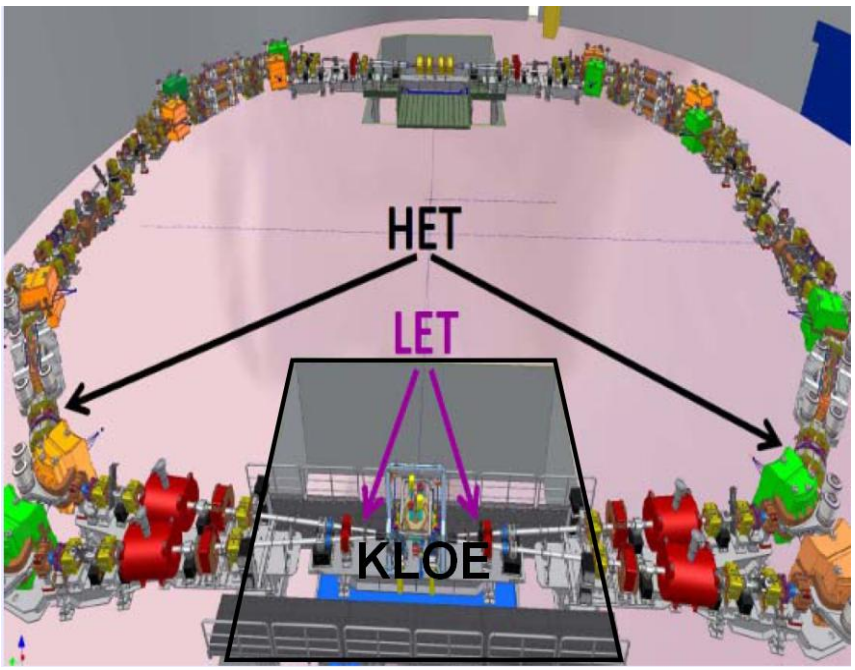


Figure 1.3: Top view of the DAΦNE storage rings showing a cut-out of the KLOE experiment, the HET and the LET positions along the beam line.

The LET detector is composed by a LYSO crystal matrix with SiPM read-out; the front end electronic is outside KLOE. The HET hodoscope is composed by two rows of scintillators with PMT read-out.

In a second phase, a light-material Internal Tracker (IT) will be installed in the region between the beam pipe and the drift chamber to improve charged vertex reconstruction and to increase the acceptance for low p_T tracks [13]. Crystal Calorimeter with Timing (CCALT) will cover the small polar angle θ region, aiming at increasing the acceptance for forward electrons/photons down to 8°. A new sampling calorimeter (Quadrupole Calorimeter with Timing, QCALT) made of scintillator tiles will be used to instrument the DAΦNE focusing system for the detection of photons coming from K_L decays in the drift chamber. The QCALT is replacing the QCAL (Quadrupole tile Calorimeter) shown in figure 1.2.

The task of QCALT calorimeter is to identify photons from $K_L \rightarrow \pi^0\pi^0\pi^0$ decays that would mimic the CP-violating decay $K_L \rightarrow \pi^0\,\pi^0$ decay if the photon would be absorbed by the DAΦNE focusing system. Figure 1.4 shows the forthcoming detector upgrades.

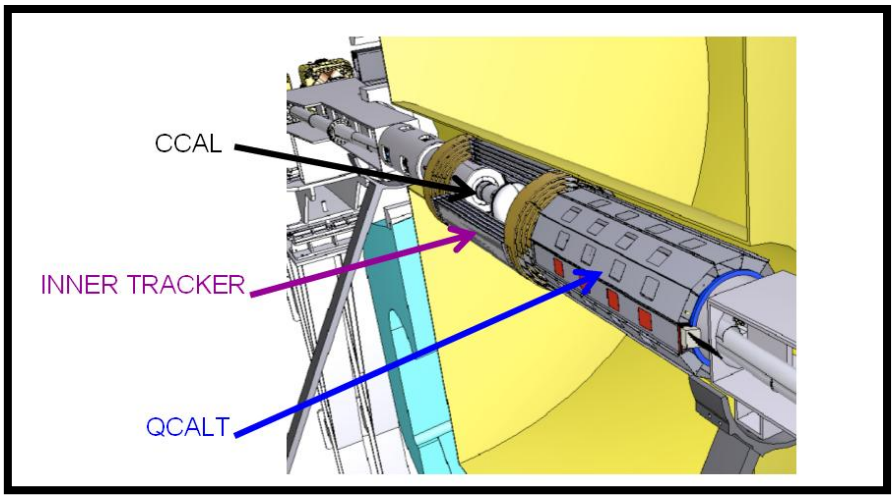


Figure 1.4: Forthcoming detector upgrades.

1.5 The KLOE electromagnetic calorimeter

The KLOE electromagnetic calorimeter [6], shown in figure 1.2, is a spaghetti like calorimeter built with lead and scintillating fibers. The lead foils are 0.5 mm thick and shaped with grooves to accommodate the scintillating fibers.

A single module is built with 200 lead-scintillating fibers layers held together by gluing. The structure is such that the response and the energy resolution are independent from the direction of the particles, thus it behaves like a homogeneous calorimeter.

The barrel modules are 4.30 m long and have a trapezoidal shape with bases 52 and 59 cm long and height 25 cm. An additional 32 modules with rectangular cross section, are wrapped around each pole piece of the magnet yoke to form the end-caps, which hermetically close the calorimeter up to ~ 98% of 4π. The fibers run parallel to the axis of the detector in the barrel, vertically in the end-caps, and are connected at both ends to light guides. The read-out is through photo-multipliers

located at both sides of the module. The arrival times of the scintillation light are used to determine the position along the module. The calorimeter read-out granularity is defined by the light collection segmentation. The fiber's direction is referred to in the following as longitudinal. The energy is determined through the measurement of the integrated charge of the photo-multipliers.

The primary functions of the electromagnetic calorimeter are the measurement of photon (electron) cluster energies and position. It also provides an accurate measurement of the time of arrival of particles.

Photons occur copiously in the decay of neutral pions, for example from $K_S K_L \rightarrow n\pi^0$'s as well as from many other products of ϕ-decays. The determination of the distance that K_L-mesons have travelled before decaying to π^0's is of crucial importance in the study of CP violation. The travelled path is obtained from a measurement of the time of arrival of photons from π^0 decays. Since neutral kaons from ϕ-mesons decaying at rest travel with a velocity $\beta \sim 1/5$, time measurements with a precision of 100 ps allow to determine the flight path of a K_L decaying in $n\pi^0$ with a precision of about 0.6 cm, for a single detected photon.

1.5.1 Clustering

The calorimeter segmentation provides the determination of the position of energy deposits in r-ϕ for the barrel and in x-z for the end-cap. A calorimeter segment is called in the following a cell and its two ends are labeled as A and B. For each cell, two time signals, $t_{A,B}$ and two amplitude signals $S_{A,B}$ are recorded from the corresponding PM's signals. The times $t_{A,B}$ (in ns) are related to $T_{A,B}$, the times in TDC counts, by the equations:

$$t_{A,B} = c_{A,B} \times T_{A,B} \qquad (1.2)$$

Where $c_{A,B}$ (in ns/TDC counts) are the TDC calibration constants. The longitudinal position of the energy deposit is obtained from the difference $t_A - t_B$.

The particle arrival time t and its coordinate z along the fiber direction, the zero being taken at the fiber center, are obtained from the times $t_{A,B}$ as:

$$t(ns) = \frac{t_A + t_B}{2} - \frac{t_A^0 + t_B^0}{2} - \frac{L}{2\upsilon} \qquad (1.3)$$

$$z(cm) = \frac{\upsilon}{2}(t_A - t_B - t_A^0 + t_B^0) \qquad (1.4)$$

Where $t^0_{A,B}$ are the overall time offsets, and L and υ are respectively the cell length (cm) and the light velocity in the fibers (cm/ns). The energy signal, E, on either side of a cell i is obtained from the signals $S_{A,B}$ as:

$$E^i_{A,B}(MeV) = \frac{S^i_{A,B} - S^{0,i}_{A,B}}{S^{mip,i}} \times k_E \qquad (1.5)$$

All signals S above are in ADC counts. $S^{0,i}$ are the zero-offsets of the amplitude scale. $S^{mip,i}$ is the response for a minimum ionizing particle crossing the calorimeter center. Dividing by $S^{mip,i}$ equation 1.5 above accounts for PM response, fiber light yield and electronics gain. k_E gives the energy scale in MeV, and it is obtained from showering particles of known energy.

In order to obtain a calorimeter response independent of the position, a correction factor $A^i_{A,B}(s)$, due to the attenuation along the fiber length, is applied. The cell energy, E_i, is taken as the mean of the determinations at both ends:

$$E_i(MeV) = \frac{E^i_A A^i_A + E^i_B A^i_B}{2} \qquad (1.6)$$

The determination of the absolute energy scale relies instead on the use of the monochromatic source of 510 MeV photons; the $e^+e^- \rightarrow \gamma\gamma$ sample. This calibration is routinely done each 200-400 nb^{-1} of integrated luminosity (i.e. approximately every 1-2 hours during normal data taking). For the timing, the relative time offsets of each channel, t_{i0}, related to the cable lengths and electronic delays and the light velocity in the fibers are evaluated every few days with high momentum cosmic rays selected with Drift Chamber information. An iterative procedures uses the extrapolation of the tracks to the calorimeter to minimize the residuals between the expected and measured times in each cell. A precision of few tens of picoseconds is obtained for these offsets.

The clustering procedure associates different hits in the calorimeter cells in a single cluster as due to the same particle. Each group collects hit cells close to each other in space and time. Among these, the cell with highest energy release is found; then, the nearest hit cells are associated to the highest one, in order to reconstruct a cluster.

The cluster energy is obtained by adding the energy released in the nearest cells:

$$E_{clu} = \sum_i E_i \qquad (1.7)$$

where i is the index of the cell number.

The cluster position is evaluated as the energy-weighted average of the cell coordinates:

$$\vec{R}_{clu} = \frac{\sum_i E_i \vec{R}_i}{\sum_i E_i} \qquad (1.8)$$

where $\vec{R_i} = (x_i, y_i, z_i)$, z_i is the cell coordinate along the fiber (see equation 1.4), and x_i, y_i are the nominal positions of the cell.

Finally, the cluster time is obtained in an analogous way:

$$T_{clu} = \frac{\sum_i E_i t_i}{\sum_i E_i} \qquad (1.9)$$

where t_i are evaluated as in equation 1.3.

1.5.2 Time, energy and spatial resolution

After the description of the calibration and monitoring procedures, the resolution of the calorimeter is here summarized.

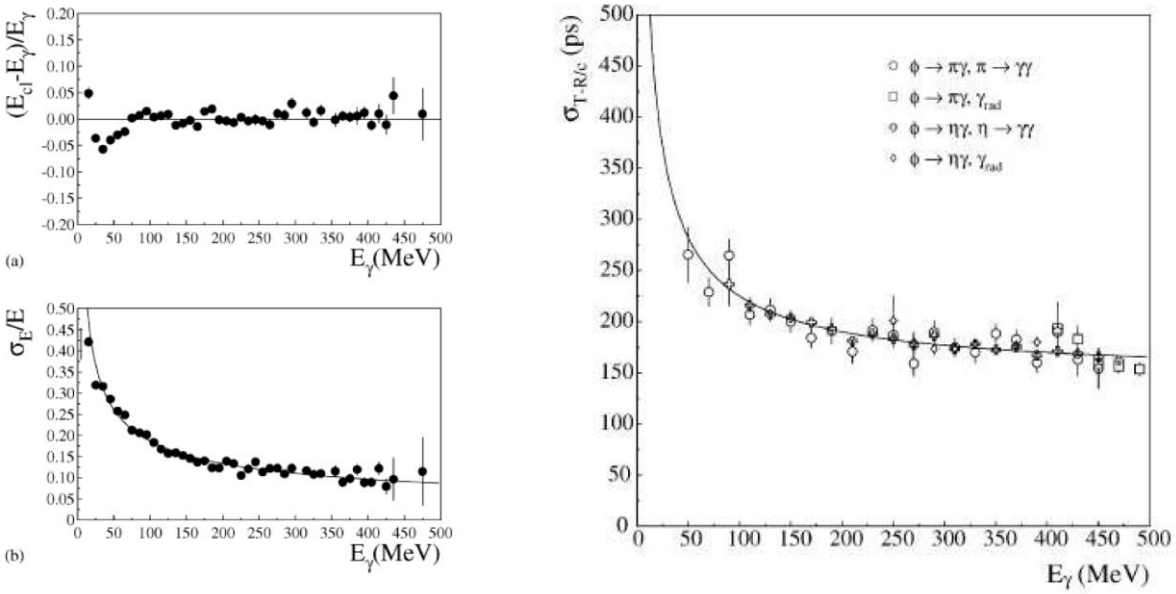


Figure 1.5: Top left: Linearity of the energy response $(E_{clu}-E_\gamma)/E_\gamma$ as a function of E_γ; Bottom left: Energy resolution as a function of E_γ; both curves are obtained with radiative Bhabha events $e^+e^-\gamma$; the fit result obtained is given by equation 1.10. Right: Time resolution as a function of E_γ for ϕ radiative decays.

The energy resolution function (see figure 1.5 on the left side) is determined with radiative Bhabha events, $e^+e^- \rightarrow e^+e^-\gamma$, where E_γ is measured by the e^+e^- DC tracking:

$$\frac{\sigma_E}{E_\gamma} = \frac{0.057}{\sqrt{E_\gamma(GeV)}} \qquad (1.10)$$

The intrinsic time resolution is $\sigma_t = 57ps/\sqrt{E_\gamma(GeV)}$ dominated by photoelectron statistics (see figure 1.5 on the right side).

A constant term determined from $e^+e^- \rightarrow \gamma\gamma$, radiative ϕ decays and $\phi \rightarrow \pi^+\pi^-\pi^0$ events has to be added in quadrature. This constant term is shared between a channel by channel uncorrelated term and a term common to all channels. The uncorrelated term is mostly due to the calibration of the time response of each cell, while the common term is related to the uncertainty of the event T_0, arising from the DAΦNE bunch-length and from the jitter in the trigger phase-locking to the

machine RF. By measuring the average and the difference of $T_{clu} - R_{clu}/c$ for the two photons in $\phi \rightarrow \pi^+\pi^-\pi^0$ events, a similar contribution of ~100 ps for the two terms has been estimated.
Thus the resolution is:

$$\sigma_t = 57\,ps/\sqrt{E_\gamma(GeV)} \oplus 100\,ps \qquad (1.11)$$

In the same way, using control samples where the photon direction is measured with the DC, the cluster position resolution function has been determined. The resolution is 1.3 cm in the coordinate transverse to the fibers and of $1.2cm/\sqrt{E_\gamma(GeV)}$ in the coordinate along the fibers. This enables to localize the $\gamma\gamma$ vertex in $K_L \rightarrow \pi^+\pi^-\pi^0$ decays with $\sigma \approx 2$ cm along the K_L line of flight, this is determined by the direction of the associated K_S meson.

1.5.3 TDC of the KLOE electromagnetic calorimeter

The main constraint for the KLOE EMC TDC design [14, 15] is to maintain the time resolution of the calorimeter response. For this, it must have excellent performances in terms of resolution, linearity and stability. The dynamic range is defined by the kinematics of kaon decays and it is fixed at 220 ns, a ~1 cm resolution implies a time resolution of 33 ps that can be obtained with a 12-bit time encoding.
Each TDC channel is built around a monolithic Time-to-Analog Converter (TAC) developed in bipolar technology, preceded by a delay circuit, as shown in figure 1.6. The TAC function principle will be described in the following chapter. In this method, the time interval is first converted into a voltage by linearly charging a capacitor with a constant current and then the voltage is held briefly to allow the analog-to-digital conversion. The digitization least significant bit is of 53 ps.
The EMC TDC works in common start mode, the start is provided by the fast first-level trigger signal T1 and the stops are provided by the KLOE EMC discriminators [16] output.

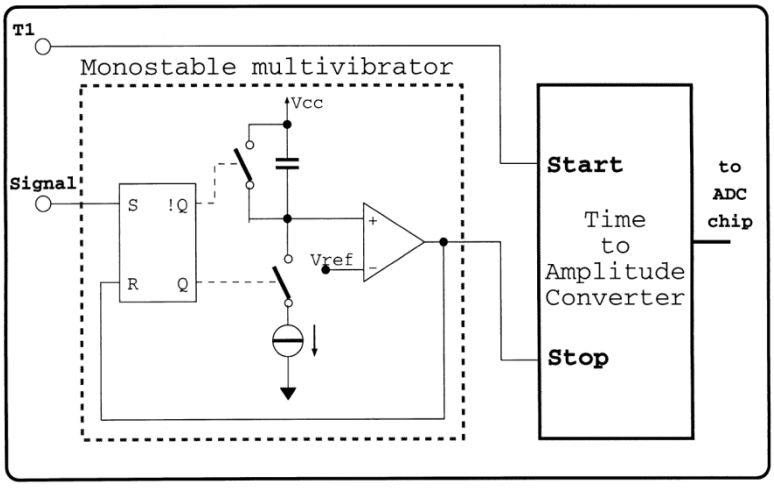


Figure 1.6: KLOE EMC TDC analog input section.

The trigger signal T1, which start the TAC conversion, is synchronized with the bunch crossing time and arrives 200-300 ns after the collision time at a rate of ~20 KHz [17]. In order to compensate for the delay of T1, the stop signals are delayed by a monostable multivibrator at the input of each channel.

The EMC TDC performances, measured on the 4880 calorimeter read-out channels, show a pedestal RMS spread less than one count, an integral non linearity of less than 0.2% of full scale and a temperature stability better than ± 0.3 count/°C.

1.6 Tile and crystal calorimeters for KLOE-2 experiment

The upgrade of the DAΦNE layout requires a modification of the size and position of the low-β quadrupoles located inside the experiment, thus asking for the realization of two new calorimeters covering the quadrupole area. To improve the reconstruction of $K_L \rightarrow 2\pi^0$ events with photons hitting the quadrupoles a calorimeter with high efficiency to low energy photon (20-300 MeV), time resolution of less than 1 ns and a space resolution of few cm, is needed. The QCALT (shown in figure 1.4) matches these requirements; it has a dodecagonal structure, 1 m long, covering the region of the new quadrupoles composed by a sampling of 5 layers of 5 mm thick scintillator plates alternated with 3.5 mm thick tungsten plates, for a total depth of 4.75 cm (5.5 X_0).

The active part of each plane is divided into twenty tiles of ~5×5 cm^2 area with 1 mm diameter plastic wavelength shifting (WLS) fibers embedded in circular grooves. Each fiber is then optically connected to a silicon photomultiplier of 1 mm^2 area, SiPM, for a total of 2400 channels.

The arrangement of the WLS fibers allows the measurement of the longitudinal *z* coordinate by time difference. Although the tiles are assembled in a way to optimize the efficiency for photons originated in K_L decays, a high efficiency is in fact also obtained for photons coming from the IP.

Moreover, the low polar angle regions (below 18°) need the realization of a dense LYSO ($Lu_{18}Y_2SiO_5$:Ce) crystal calorimeter with very high time resolution performances to extend the acceptance for multiphotons events, the CCALT (shown in figure 1.4). The most important characteristics of these crystals are a very high light yield, a time emission, τ, of 40 ns, high density and $1/X_0$ without being hygroscopic. The project consists in a dodecagonal barrel for each side of the interaction region, composed by LYSO crystals (2x2x13 cm^3) read-out using avalanche photodiodes (APD). This allows to increase the acceptance for forward electrons/photons down to 8°.

1.7 Time measurements in KLOE-2

The bunch identification can be obtained using a TDC with a resolution better than 0.5 ns since the inter bunch time difference is 2.715 ns. In this thesis I describe a TDC architecture that allows a resolution in the range of 20 ps. With such a resolution we should be able to improve the signal/background ratio by using a constrained fit on the kinematic of the event. The dynamic range of the described TDC is about 8 seconds which is far more than we need in KLOE since the K_L lifetime is about 50 ns.

Moreover such a TDC is based on a flash architecture. This implies a dead time of 12.7 ns. Such a device can therefore be used in high trigger rate environment like Super B Factories where the estimated trigger rate is about 150 kHz at a luminosity of 10^{36} cm^{-2} s^{-1}.

Chapter 2

Review of methods for time interval measurements

2.1 Introduction

Time interval measurements between two or more physical events are often required in many applications in High Energy and Nuclear Physics. Such experiments are aimed in mean life-time measurements of excited states, angular correlation functions, time-of-flight measurements and particle identification. Usually the time interval is measured between the leading edges of a START and a STOP signal. These signals may be generated by the front-end electronics used to extract the timing information coming from a particle detector. Particles interacting with the detectors generate electrical signals (charge, current or voltage) which have to be measured with the best accuracy, stability and resolution consistent with the experimental requirements. The detector signals are processed by the front-end electronics that usually is built by amplifiers, shaper circuits and discriminators. The front-end electronics deliver the START and STOP signal to the Time-to-Digital Converter (TDC) that performs the conversion of the time interval into a binary word, which can be displayed in a decimal form. So the accuracies and resolution of a time measurement in physics experiments takes into consideration the contribution from all the components of the system: the detector, the front-end electronics and the TDC. Figure 2.1 shows a simplified view of a TDC with two separate inputs of START and STOP.

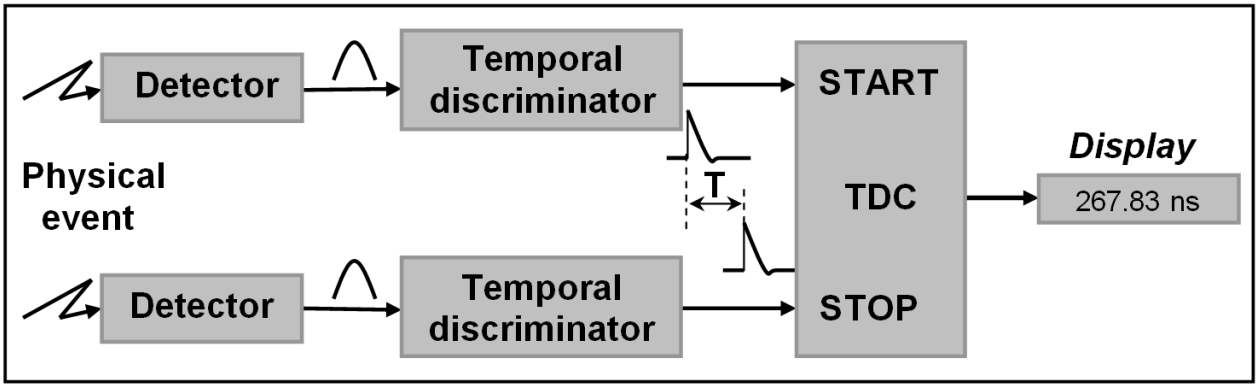


Figure 2.1: Principle of a time interval measurement.

2.2 Conversion basics

The characteristic parameters of a TDC are:

- The range of measurements, which is the largest time interval that can be measured.
- The standard measurement uncertainty, expressing the time interval resolving capability of a TDC, i.e. the standard deviation of the measurements distribution around the mean value, when a constant time interval is measured several times.
- The resolution, which is the least significant bit of the binary word read and then the smallest time interval measured.
- The reading speed or how fast is the tool to produce the measurements result. This parameter is important when measurements are made in continuous way at high frequencies and with real time readings.
- Non-linearity of the time-to-digital conversion: differential and integral, expressing the deviation from the ideal behaviour of the converter.

Figure 2.2 (left) shows the ideal transfer function of a TDC, which displays the conversion of a time interval in a binary word, each corresponding to one step of the curve; this will inevitably include [18] a quantization of the measurement. Figure 2.2 (right) shows the real transfer function from which is noticed the deviation from the ideal case that is usually measured by the differential and integral non-linearity.

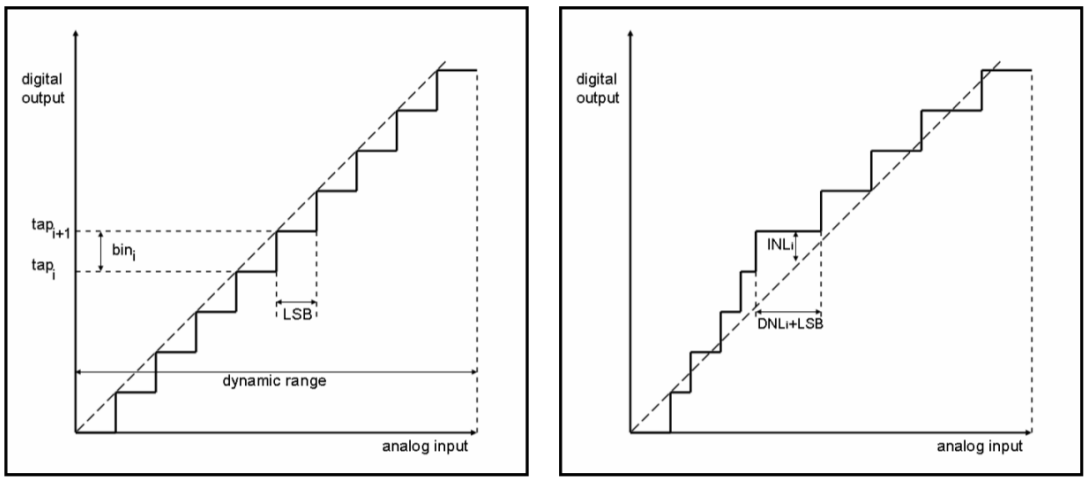


Figure 2.2: TDC transfer function. Left: ideal case. Right: real case.

The differential non-linearity (DNL) is:

$$DNL_i = \frac{LSB_i - \overline{LSB}}{\overline{LSB}} \tag{2.1}$$

Where LSB_i is the i-th time interval corresponding to the Least Significant Bit of the i-th bin. The DNL expresses the deviation of the bin width from its ideal value. So there is a difference between

the bin width for a given binary value output and the average width of the bin calculated over the entire measuring range; the difference is then divided by the average value of the bin.
The integral non-linearity is:

$$INL_j = \sum_{i=1}^{j} \frac{1}{M} \frac{LSB_i - \overline{LSB}}{\overline{LSB}} \tag{2.2}$$

The INL is determined for a bin j from the sum of previous differential non-linearity until the bin j, this sum is divided by the total number M of bin of the TDC. To describe the linearity error by a single value, usually the maximum value of INL_j or $INL_{j\ max}$ ($1 \leq j \leq M$) is selected, which represents the worst case.

2.3 Precision frequency standards

Several different types of devices are used to generate high precision clock signals, as uncompensated crystal oscillators (XO), temperature-compensated crystal oscillators (TCXO), oven-controlled crystal oscillators (OCXO) or atomic frequency standards; the progress achieved in terms of performance of these devices leads to the characterization of their frequency stability.
The output voltage of a sinusoidal generator can be written in the following form:

$$u(t) = (U_0 + \varepsilon(t))\sin(2\pi\nu_0 t + \phi(t)) \tag{2.3}$$

U_0 is the nominal value of the amplitude and ν_0 the nominal value of the frequency. In the following, is assumed that the amplitude fluctuation $\varepsilon(t)$ is negligible in comparison with U_0 and is considered only the phase fluctuation $\phi(t)$. The Greek letter ν is used to indicate the signal frequency while the Latin symbol f is used as frequency variable in the Fourier representation of the signal. The frequency of the sinusoidal voltage is equal to:

$$\nu(t) = \nu_0 + \frac{1}{2\pi}\frac{d\phi}{dt} = \nu_0 + \nu_\nu \tag{2.4}$$

and is the sum of a constant nominal value ν_0 and a variable term:

$$\nu_\nu = \frac{1}{2\pi}\frac{d\phi}{dt} \tag{2.5}$$

The normalized frequency offset from the nominal frequency of the signal is designated by y(t) and defined as follows:

$$y(t) = \frac{\nu_\nu}{\nu_0} = \frac{1}{2\pi\nu_0}\frac{d\phi}{dt} \tag{2.6}$$

Another useful quantity is the time integral of y(t):

$$x(t) = \int_0^t y(t')dt' = \frac{\phi(t)}{2\pi\upsilon_0} \tag{2.7}$$

and also:

$$y(t) = \frac{dx}{dt} \tag{2.8}$$

The normalized frequency offset y(t) and the phase-time x(t) are to be interpreted as random processes and can be described by statistical method.

Most real oscillators not only exhibit random frequency variations about a nominal average but also a systematic frequency drift with time:

$$y(t) = y_r(t) + at + y_0 \tag{2.9}$$

and also:

$$x(t) = x_r(t) + \frac{a}{2}t^2 + y_0 t \tag{2.10}$$

where *a* is a normalized aging coefficient, y_0 an initial offset and y_r, x_r the truly random processes. It's assumed that the mean value of y_r over the period of observation is equal to zero, furthermore it's always possible to subtract the drift term *at* and y_0 from the data; then is assumed that also y(t) have a zero mean value over the time of observation.

The result of a frequency measurement is always obtained as an average over a finite time interval τ, any sample is of the form:

$$\overline{y_k}(t_k, \tau) = \frac{1}{\tau}\int_{t_k}^{t_k+\tau} y(t)dt = \frac{1}{\tau}(x(t_k+\tau) - x(t_k)) \tag{2.11}$$

The measurements are taken at regular time intervals $T = t_{k-1} - t_k$, with dead time $T - \tau$. For a series of N measurements the results are:

$$\overline{y_k}(t_k, \tau) = \overline{y_1},\ \overline{y_2}, ..., \overline{y_N} \tag{2.12}$$

The mean value is:

$$\langle \overline{y_k} \rangle_N = \frac{1}{N}\sum_{k=1}^{N} \overline{y_k} \tag{2.13}$$

and the variance of the sample of N values:

$$\sigma_y^2(N, T, \tau) = \frac{1}{N-1}\sum_{k=1}^{N} (\overline{y_k} - \langle \overline{y_k} \rangle_N)^2 \tag{2.14}$$

According to the assumption made above, the limit should be:

$$\lim_{N\to\infty} \langle \overline{y_k} \rangle_N = 0 \tag{2.15}$$

whereas the limit

$$\lim_{N\to\infty} \sigma_y^2(N, T, \tau) = \sigma^2(\tau) \tag{2.16}$$

should tend to the variance $\sigma^2(\tau)$ of the process if such a limit exists. Even after elimination of any initial offset and linear drift, it is found that the sample variance $\sigma_y^2(N,T,\tau)$ depends on all of the three variables N, T and τ. The sample variance defined in (2.14) is therefore not useful to describe experimental data in the time domain. A possible solution to this problem has been proposed by D.W. Allan [19] and J.A. Barnes [20] who have shown that for limited values of N, T and τ the limit:

$$\langle \sigma_y^2(N,T,\tau) \rangle = \lim_{M \to \infty} \frac{1}{M} \sum_{i=1}^{M} \sigma_{yi}^2(N,T,\tau) \tag{2.17}$$

exists in many cases of interest where the limit (2.16) does not exist. The average of the sample variance as defined in (2.17) is referred as Allan variance.

The behaviour of y(t) in the frequency domain is described by its spectral density $S_y(f)$ which is defined in the usual way as the Fourier Transform of the auto-covariance $R_y(\tau)$, as follows:

$$R_y(\tau) = \lim_{T \to \infty} \frac{1}{T} \int_0^T y(t') y(t'+\tau) dt' \tag{2.18}$$

Then the spectral density is defined according to the Wiener-Khintchine relation [21] as:

$$S_y(f) = 4 \int_0^{\infty} R_y(\tau) \cos 2\pi f \tau d\tau \tag{2.19}$$

The relation between the spectral density $S_y(f)$ and the general form of the Allan variance is [22,23]:

$$\langle \sigma_y^2(N,T,\tau) \rangle = \frac{N}{N-1} \int_0^{\infty} S_y(f) \, |H(f)|^2 df \tag{2.20}$$

where:

$$|H(f)|^2 = \frac{\sin^2 \pi f \tau}{(\pi f \tau)^2} \left(1 - \frac{\sin^2 \pi r f \tau N}{N^2 \sin^2 \pi r f \tau} \right) \tag{2.21}$$

and $r = T/\tau$.

The main reason why the Allan variance has become a useful parameter for the characterization of frequency stability is that the integral of (2.20) has the property of existing even for some cases of non-integrable (infinite power) spectral densities.

The Allan variance for N = 2 has another advantage which is the extreme simplicity of computation from measured data:

$$\langle \sigma_y^2(2,T,\tau) \rangle = \frac{1}{2} \langle (\bar{y}_{k+1} - \bar{y}_k)^2 \rangle \tag{2.22}$$

In several applications it is possible to make the measurements with negligible dead-time. It then can be assumed that T = τ. The N=2, T=τ Allan variance has been proposed as a recommended measure for frequency stability in the time domain. It is usually designated by:

$$\sigma_y^2(\tau) \equiv \langle \sigma_y^2(2,\tau,\tau) \rangle \tag{2.23}$$

Some authors use the term Allan variance for this special case only.

The types of noise observed on the output signal of an oscillator can be represented most suitably by means of the spectral density $S_y(f)$. In practice, these random fluctuations can often be represented by the sum of five independent noise processes, and hence:

$$S_y(f) = \begin{cases} \sum_{\alpha=-2}^{2} h_\alpha f^\alpha & \text{for} \quad 0 < f < f_h \\ 0 & \text{for} \quad f \geq f_h \end{cases} \tag{2.24}$$

where h_α's are constants, α's are integers, and f_h is the high frequency cut-off of a low pass filter. High frequency divergence is eliminated by the restrictions on f in this equation.

In the special case of N= 2, T = τ the Allan variance is:

$$\sigma_y^2(\tau) \equiv \langle \sigma_y^2(2,T,\tau) \rangle = \frac{2}{\pi\tau} \int_0^\infty S_y\left(\frac{u}{\pi\tau}\right) \frac{\sin^4 u}{u^2} du \tag{2.25}$$

where $u=\pi f\tau$.

Then, the relationship between the Allan variance and every term of the form $h_\alpha f^\alpha$ is:

$$\sigma_y^2(\tau) = \frac{2h_\alpha}{(\pi\tau)^{\alpha+1}} \int_0^{\pi\tau f_h} u^{\alpha-2} \sin^4 u du \tag{2.26}$$

that is:

$$\sigma_y^2(\tau) = K_\alpha \tau^\mu \tag{2.27}$$

with μ=-α-1 and $K_\alpha = \frac{2h_\alpha}{\pi^{\alpha+1}} \int_0^{\pi\tau fh} u^{\alpha-2} \sin^4 u du$.

Information about the spectral densities $S_y(f)$ can be obtained from time-domain measurements of $\sigma_y(\tau)$ versus τ on double logarithmic scale, this kind of plot yields segments of straight lines in the ranges of τ where one of the various term $h_\alpha f^\alpha$ or $K_\alpha \tau^\mu$ dominates.

The widely used standard frequency sources are [24][25]:

- caesium-beam resonators;
- hydrogen masers;
- hydrogen storage beam tube;
- methane saturated absorption cells;
- rubidium vapour cells.

Furthermore, quartz-crystal oscillators, without being accurate frequency standards, are of high importance as slave oscillators in all radio frequency standard.

The caesium atomic beam is produced from a heated oven containing liquid caesium. The first state selector allows only atoms of a selected hyperfine state to pass through the interaction region, where

transitions are produced by a pair of separated oscillating fields (Ramsey method) in a microwave cavity (ν_0=9.2 GHz). Simultaneously a uniform weak magnetic field (C-field) is applied in order to separate the different sublevels of the hyperfine state, so the transitions occur only between the two levels (m_F=0), where the Zeeman effect is purely quadratic. The second state selector allows only atoms that have completed the transition to the other hyperfine state to be detected. The caesium atoms are detected by surface ionization on a hot-metal ribbon. Usually the ion current is amplified by means of a secondary electron multiplier. As a function of excitation frequency, the output current shows a sharp resonance peak. Figure 2.3 shows the principle of caesium beam frequency standard.

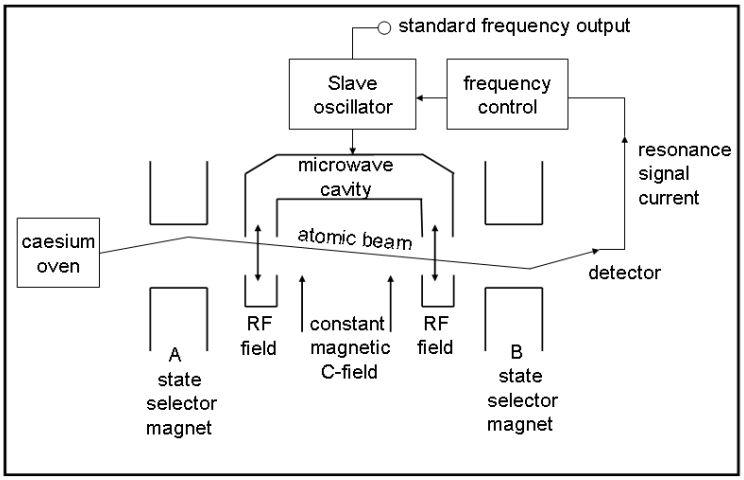


Figure 2.3: Principle of caesium beam frequency standard.

In the Hydrogen masers, the atomic hydrogen is produced in a radio frequency discharge source and the beam is formed in a collimator. Atoms in the upper hyperfine state are focused into a coated storage bulb by means of a multipole magnet. The storage bulb is located in the uniform radio frequency field region of a high Q cavity. A weak uniform magnetic field is applied for the same reason as in a caesium tube. The condition of oscillation depends on various relaxation process, the flux ratio of atoms in the desired and undesired states, and the loaded Q of the tuned cavity. Figure 2.4 shows the principle of hydrogen maser frequency standard.

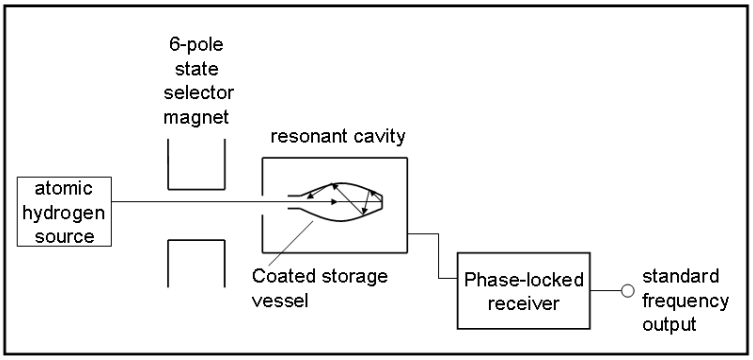


Figure 2.4: Principle of hydrogen maser frequency standard.

Hydrogen storage beam tubes combine the advantages of the passive resonator with those of hydrogen atom storage in a coated bulb. Source and first state selector are similar to those of a hydrogen maser. An output collimator, a second state selector and hydrogen atom detector are added to the storage bulb. Figure 2.5 shows the principle of hydrogen storage beam frequency standard.

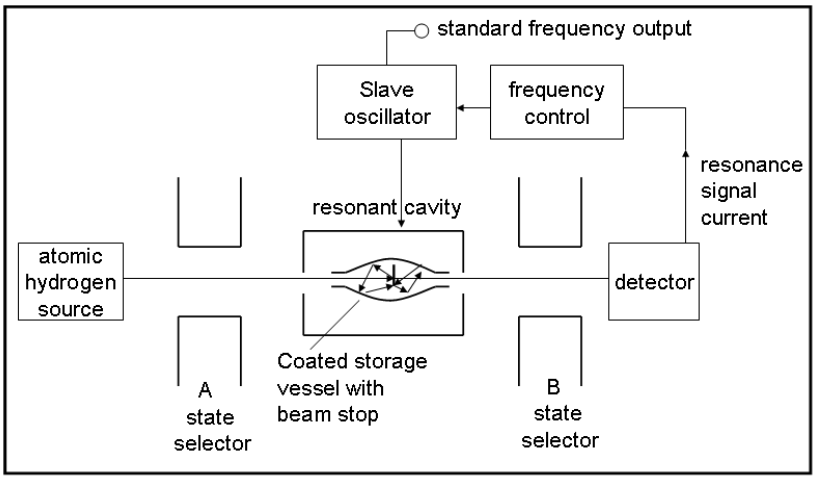


Figure 2.5: Principle of hydrogen storage beam frequency standard.

Figure 2.6 shows the principle of rubidium vapour cell frequency standard. A light beam from an ^{87}Rb lamp, filtered by a vapour cell containing ^{85}Rb, depopulates one of the two hyperfine levels of ^{87}Rb atoms stored in another cell which is located inside a cavity. Figure 2.7 shows the simplified energy level diagram in which the resonance radiation of the ^{87}Rb lamp is filtered by means of the ^{85}Rb isotope absorption in such a way that there are more transitions from the $5S_{1/2}$ F=1 level up to the $5P_{3/2}$ level than from the $5S_{1/2}$ F=2 level. The lower ground state hyperfine level $5S_{1/2}$ F=1 is thus depopulated. Absorption on the 7800 angstrom wavelength then ceases until the application of the 6834 MHz microwave radiation to the cavity.

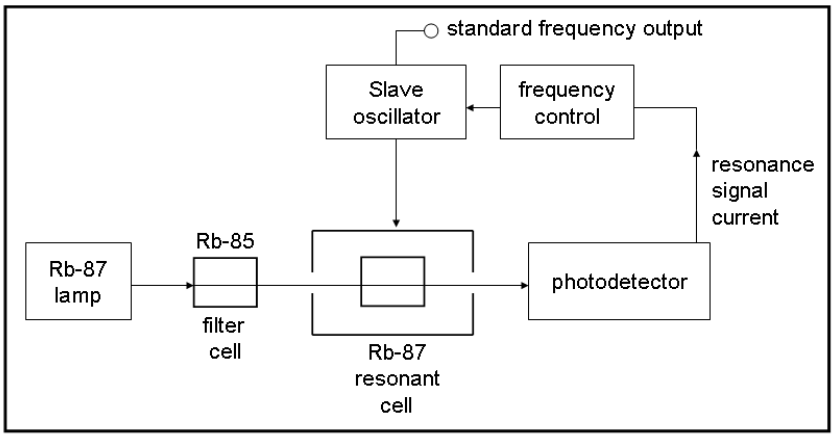


Figure 2.6: Principle of rubidium vapour cell frequency standard.

The latter repopulates the lower level by means of induced transitions from the F=2 down to the F=1 level and absorption of the 7800 angstrom pumping radiation is again observed at the photodetector, which thus provides the resonance signal for locking the slave oscillator. With high levels of pumping light, appropriate choice of buffer gases, and high Q cavity, maser oscillation can be obtained. In practical applications, however, the passive mode of operation is the only one used. This is the simplest and least expensive type of atomic frequency standard and it has found wide acceptance for those applications where its ageing with time is non inconvenience. An even simpler variety, using natural rubidium in a resonance cell without additional filter cell is also used.

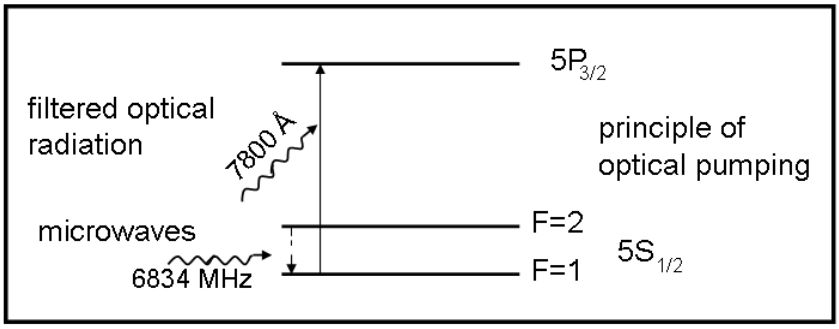


Figure 2.7: Simplified energy level diagram.

Methane saturated absorption cell is a high accuracy frequency standard in the infrared region. A gas cell filled with methane is mounted with a ^{3}He-^{20}Ne gain cell between the two mirrors of a laser cavity. The He-Ne laser can be made to oscillate at a frequency of approximately 88 THz (wavelength 3.39 μm) which coincides with a resonance of the methane molecule. With appropriate methane pressure, strong absorption occurs over the whole range of oscillation of the laser. Methane molecules in the cell interact with both running waves forming the standing wave pattern in the Fabry-Perot resonator of the laser system.

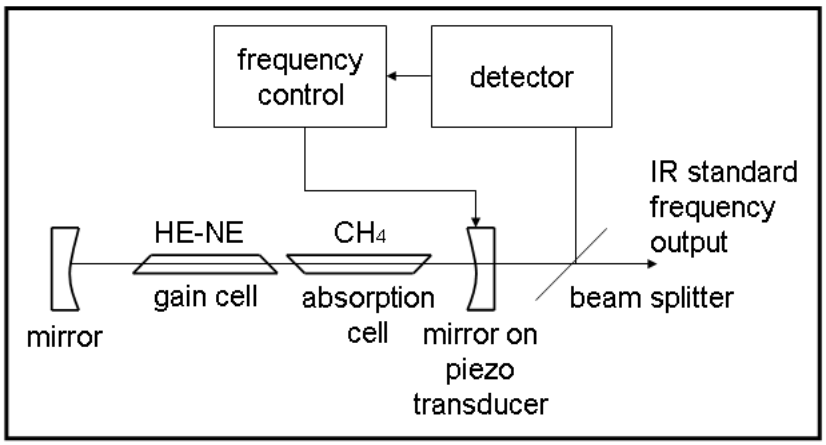


Figure 2.8: Principle of Methane saturated absorption frequency standard.

Molecules having arbitrary velocities are perturbed at two different frequencies because of the first order Doppler shift which is of opposite sign for each running wave. For the molecule moving in a direction perpendicular to the laser beam, the Doppler shift vanishes. These molecules are perturbed by a signal at twice the amplitude without Doppler shift. If the intensity of the laser radiation is sufficiently high and its frequency adjusted, the lower energy level of the molecular transition is depopulated. Additionally, photons will be re-emitted coherently through induced transitions. Therefore, less energy will be absorbed from the laser beam if its frequency is that corresponding to the molecular transition. This phenomenon is called saturation and the dip in the absorption line profile known as the "Lamb dip". The resonance signal is observed by means of a photodetector. The frequency of the He-Ne laser is modulated for scanning the resonance by means of a piezoelectric transducer moving one of the laser mirrors. The average frequency is locked to the methane resonance by means of an electronic servo system.

Table 2.1 shows the state of the art in the accuracy capability of crystal oscillators and commercial atomic frequency standards [26]. Figure 2.9 shows a time-domain measurements of $\sigma_y(\tau)$ versus τ of precision commercial and laboratory frequency standards [26].

device	stability @ 1 s	stability @ 1 day	stability @ 1 year
OCXO	$5x10^{-10}$ to $5x10^{-12}$	$5x10^{-9}$ to $5x10^{-10}$	$1x10^{-6}$ to $5x10^{-8}$
Rb	$3x10^{-11}$ to $5x10^{-12}$	$1x10^{-13}$	$1x10^{-10}$
Cs	$6x10^{-11}$ to $5x10^{-12}$	$2x10^{-13}$ to $3x10^{-14}$	$3x10^{-12}$
H (passive)	$2x10^{-12}$	$1x10^{-14}$	$<1x10^{-12}$

Table 2.1: Accuracy capability of crystal oscillator and commercial atomic frequency standard.

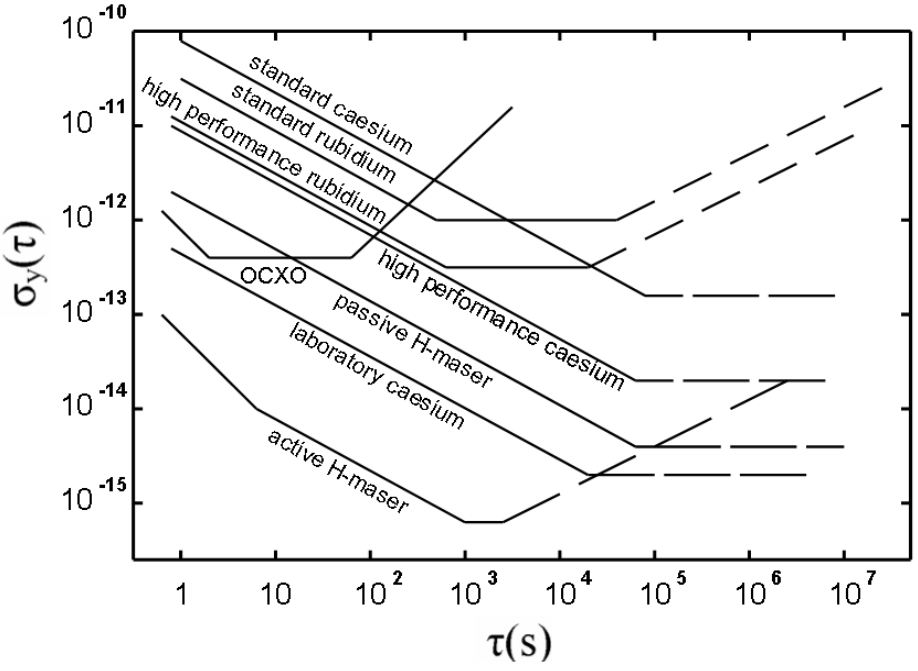


Figure 2.9: A frequency stability diagram of precision frequency standards.

2.4 The Nutt method

The Nutt method [27] combines different time measurements with different ranges and accuracies into one; it's usually used when a large linear dynamic range and high resolution are needed simultaneously. Figure 2.10 shows the measurement of a time interval with the Nutt method.

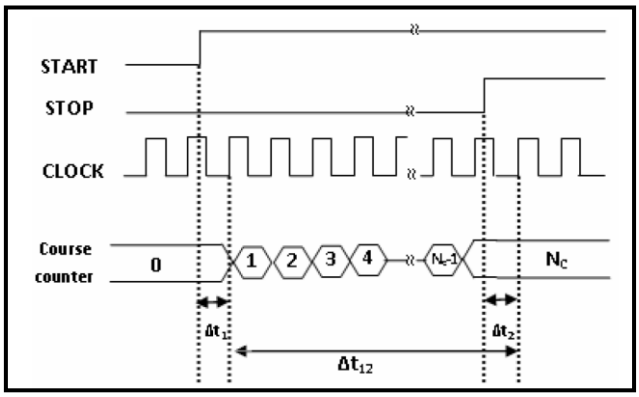


Figure 2.10: Measurement of a time interval with Nutt method.

The time measurement consists of three phases; first, the time interval Δ_{t1} between the rising edges of the START signal and the subsequent reference clock edge is measured using a fine TDC. The same procedure is exploited to measure the time interval Δ_{t2} between the rising edges of the STOP signal and the subsequent reference clock. The coarse TDC measures the time interval Δ_{t12} between the two rising edges of the reference clock immediately following the START and STOP signals. The time interval between the START and STOP signals is:

$$\Delta t = \Delta_{t1} + \Delta_{t12} - \Delta_{t2} \qquad (2.28)$$

So there are two different kind of measurements: coarse and fine. The coarse measurement has a resolution usually given by the clock system period. The fine measurement improves the TDC resolution within the clock period. The fine conversion dynamic ranges Δ_{t1} and Δ_{t2} are limited to only one reference clock cycle and usually are between 10 ns and 200 ns. Figure 2.11 shows a simplified block diagram of such interpolating TDC. It contains two interpolator fine TDCs and a coarse TDC.

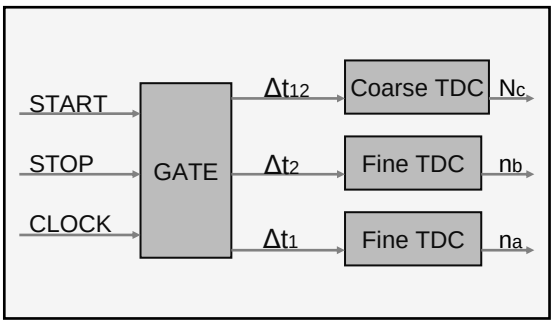


Figure 2.11: Simplified block diagram of the Nutt interpolating method.

2.5 TDC architectures

In the following, a review of the most relevant TDC architectures is described [28]; the principal methods of time interval measurements are:

- time interval measuring system based on counter techniques,
- time-stretching followed by a counter,
- time-to-voltage conversion followed by analog-to-digital conversion,
- Vernier techniques,
- Time-to-digital conversion using digital delay lines.

Counter techniques offer a very large dynamic range, but the resolution of the measurement is limited by the maximum frequency of the clock signal. In order to improve the time resolution of the measuring system the time acquisition process have to be based on the Nutt method achieved with a two stage interpolation.

The techniques used to achieve a fine time measurement can be roughly classified as analog (time-stretching and time-to-voltage conversion) and digital (Vernier and digital delay line techniques).

Usually the analog methods are more difficult to implement in the integrated circuit technology, they have longer conversion time and they are more sensitive to the physical operating parameters like on-chip power supply voltages and die temperatures. Digital methods are easier to implement in the integrated circuit technology, they have faster conversion time and show a better stability.

2.6 The counter method

The measurement principle of the counter method is based on counting the cycles of a stable reference oscillator [29]. A START and STOP pulse mark the moments when the counter is sampled, the difference between these two samples is the measurement of the time interval. Time interval of microseconds or longer can be measured with a moderate resolution, equal to a clock period. Such design requires very fast counter, which are rather expensive devices. A very high speed counter can be obtained in the structure of a linear feedback shift register (LFSR) or simple Gray code counters. The LFSR has the disadvantage of the pseudo-random output code, which has to be converted to the natural binary or BCD code. Gray counter are less sensitive to the metastability in counter's register when the START or STOP signals arrive [30], in fact in this case only one bit toggles for each clock cycle. Further measure improvements are possible through use of phase shifting to obtain a subdivision of the clock period, i.e. several counter synchronous to different phases of the same clock can be used to increase the resolution. The time measurement can be interpolated from the results of all the counters.

When using the counter method, the measurement is asynchronous with the time base, so it can begin and end at any time inside the clock period T_0. A time interval T, can be written as $T=(N_c+f)T_0$, where N_c in an integer and $0<f<1$. In an ideal case the measured time interval has two possible binary values, N_c and N_c+1, depending on the position of the time interval within the rising edges of the clock signal. So the maximum quantization error of a single measurement may be almost T_0.

Averaging can be used to improve the accuracy of counter measurements taking a series of measurements of a constant and asynchronous time interval [31]. The measured time can give two binomially distributed results, N_c counts with probability (1-f) and N_c+1 counts with probability f.

The standard deviation of the binomial probability distribution is:

$$\sigma = T_0\sqrt{f(1-f)} \tag{2.29}$$

Figure 2.12 shows the standard deviation of measurements as function of f, the fractional part of the quotient T/T_0. The maximum single-shot precision of 0.5 T_0 can be measured when f=0.5. When f=0 the single shot precision is ideally zero, so the measurements are collected in N_c counts, while if f=1, the measurements are collected in N_c+1 counts.

The average standard deviation can be obtained by integrating the standard deviation over one T_0 period, it yields:

$$\sigma_{av} = \frac{\pi T_0}{8} \cong 0.39T_0 \tag{2.30}$$

The counter resolution can be improved by taking a series of measurements and averaging the results; the average standard deviation is:

$$\sigma_{N\,av} = \frac{\pi T_0}{8\sqrt{N}} \cong 0.39\frac{T_0}{\sqrt{N}} \tag{2.31}$$

The main problem with time interval averaging is the long time it takes to make a reading which cannot fit the needs of high speed systems.

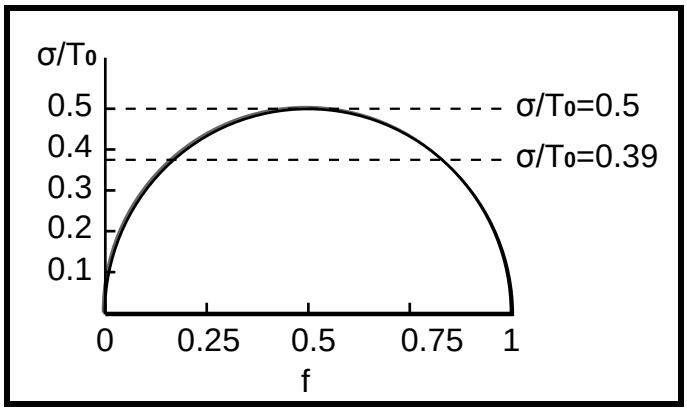


Figure 2.12: Standard deviation of measurements as function of the fractional part f.

2.7 Time-stretching

The method of time-stretching is probably the most common technique used for time interval measurements. It involves taking a capacitor and charging it with a constant current during the time interval T and then discharging it with a much smaller current. The capacitor, therefore, charges up quickly, but discharges slowly. Figure 2.13 shows the simplified circuit of this current integration technique.

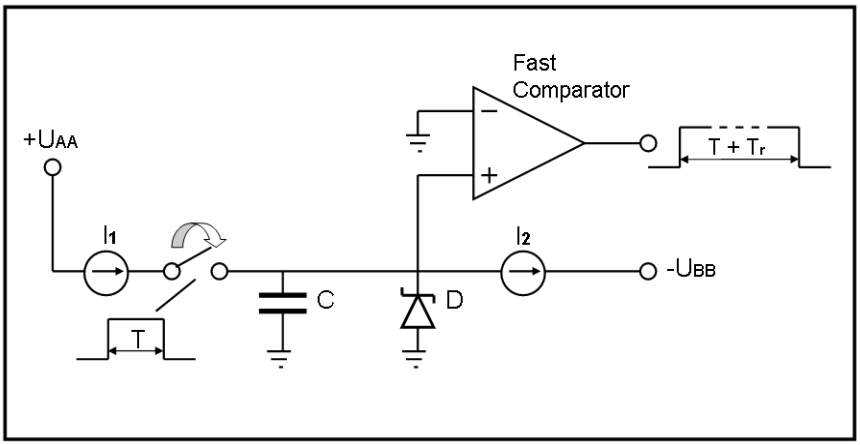


Figure 2.13: Simplified circuit for time-stretching.

In the steady-state the diode D conducts a current I_2. During the time interval T, the capacitor C is charged linearly with a constant current (I_1-I_2). The charge stored in the capacitor is thus proportional to T, so $\Delta Q = (I_1\text{-}I_2)\ T$. Then after the time interval T, the capacitor is discharged through the smaller current I_2. The discharging time is T_r, so $\Delta Q = I_2\ T_r$, then:

$$(I_1 - I_2)T = I_2 T_r \qquad => \qquad T_r = \frac{(I_1 - I_2)}{I_2} T = KT \tag{2.32}$$

where K is the stretching factor.

Then, the discharging time is $T_r = KT$ and the total time $(T + T_r) = (K+1)T$.

Figure 2.14 shows the plot of the charge and discharge of the capacitor as function of the time, it is clear that this method involves the conversion of a small time interval in a bigger one in order to improve the time measurements realized by the counter method. The voltage across the capacitor is $\Delta V = \frac{\Delta Q}{C}$, so a fast comparator can be used to detect the pulse over threshold in order to deliver the total time ($T+T_r$); finally this time interval is measured by using a simple counter.

$$T + T_r = (K+1)T = NT_0 \tag{2.33}$$

N is the counter counts number and T_0 is the period of the counter clock signal. Then the measured result is:

$$T = N\frac{T_0}{K+1} \tag{2.34}$$

The time-stretching technique provides an effective resolution equal to $\frac{T_0}{K+1}$.

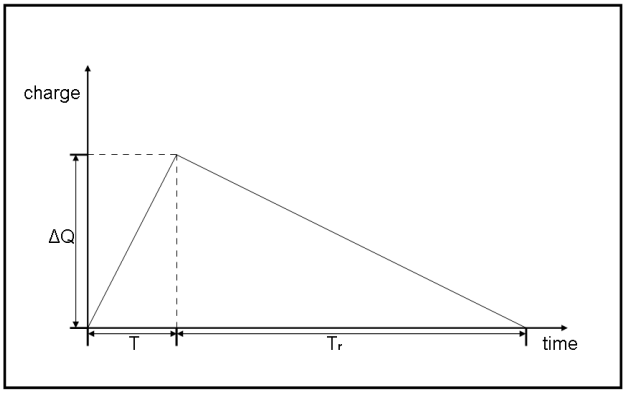


Figure 2.14: Plot of the charge and discharge of the capacitor versus time.

The time-stretchers are usually built with discrete circuits at low cost. The best resolution obtained with this method is about 1 ps with the use of a two-stage time stretchers [32,33].
The main advantage of a high resolution is a small quantization error, which can be neglected. The drawback of time-stretching is the long time required for the conversion, equal to KT and limiting the maximum frequency of the measures.

2.8 Time-to-voltage conversion

Time-to-voltage conversion is another analog method commonly used; it is similar to the time-stretching technique, but in this method the value of the voltage across the capacitor is directly read by an Analog-to-Digital Converter (ADC). The time interval is first converted into a voltage by linearly charging a capacitor with a constant current and then the voltage is held briefly to allow the analog-to-digital conversion. Figure 2.15 shows a simplified circuit of the conversion of the time interval to amplitude followed by the analog-to-digital conversion stage.

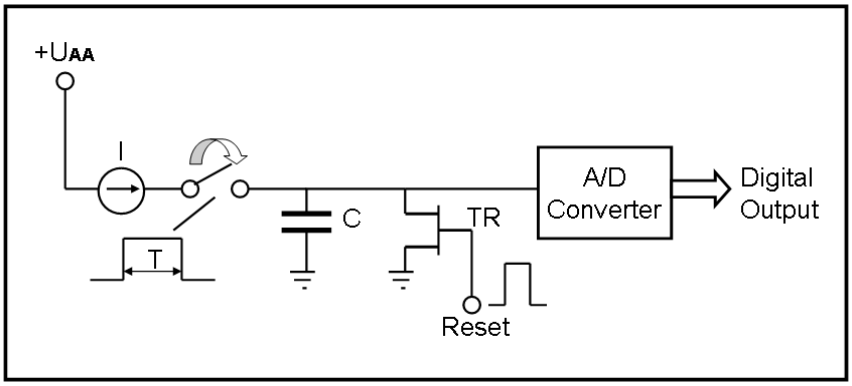


Figure 2.15: Simplified circuit for time-to-voltage converter.

The voltage across the capacitor is proportional to the time interval:

$$\Delta V = \frac{I}{C} T \qquad (2.35)$$

After the measure the capacitor is rapidly discharged in order to minimize the dead time between different measurements. The conversion time of this method is related to that of the ADC used.

Figure 2.16 shows the plot of the voltage across the capacitor versus time.

This method has been used in many designs built with discrete and integrated circuits [34-38]. However large-scale integration is difficult due to the characteristics of the process parameters and the noise sensitivity of the architecture.

As the time-stretcher method, the time-to-voltage conversion can reach picoseconds resolution. The constraint of these current integration technique is the limited dynamic range given by the maximum voltage to which the capacitor can be charged (i.e. the supply voltage).

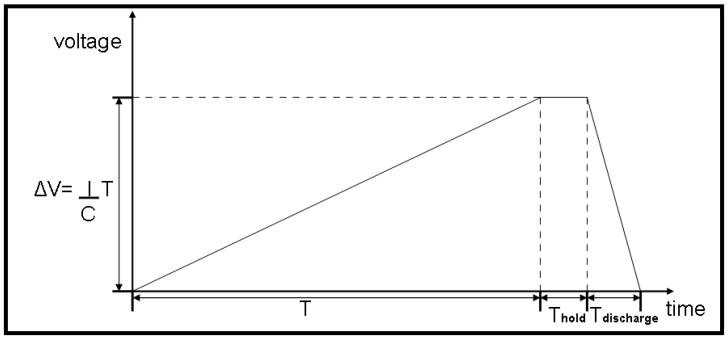


Figure 2.16: Plot of the voltage across the capacitor versus time.

2.9 The Vernier method

Pierre Vernier (19 August 1580 at Ornans, France – 14 September 1637 same location) was a French mathematician and instrument inventor. He was inventor and eponym of the Vernier scale used in measuring devices.

The Vernier method is an extension of the counter technique; it is based on a digital time-stretching approach. The principle of operation is the same as the Vernier calibre used to measure length. Figure 2.17 shows the simplified block diagram of the Vernier time interval digitizer. This converter uses two gated oscillators generating stable reference signals with slightly different periods. The frequencies are:

$f_1 = \frac{1}{T_1}$ lower frequency,

$f_2 = \frac{1}{T_2}$ higher frequency,

T_1 and T_2 are the clock periods.

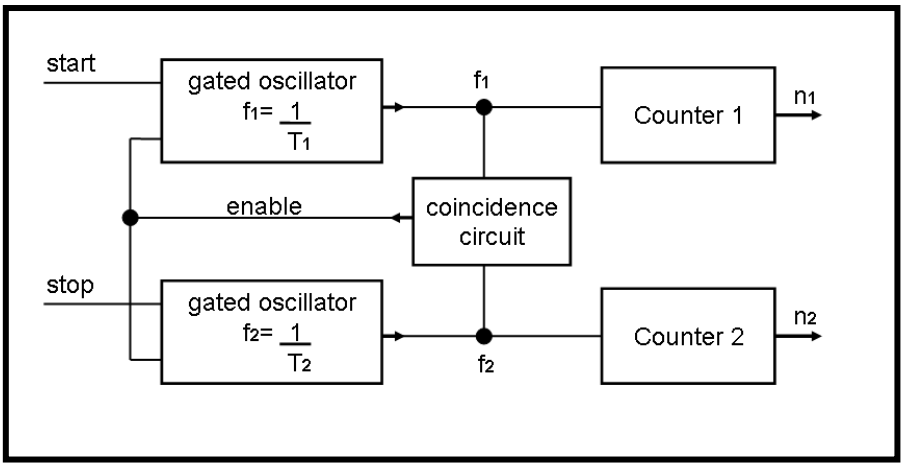


Figure 2.17: Simplified block diagram of the Vernier method.

Figure 2.18 shows the timing diagram of the Vernier method. The oscillators are gated on by the rising edges of the START and STOP pulses. T is the time interval to be measured. The phase of the clock signal generated by the STOP oscillator gradually catches up with the phase of the clock signal generated by the START oscillator. The phase alignment of the signals rising edges is detected by a coincidence circuit and the oscillators are then disabled. The number of clock cycles n_1 and n_2 elapsed between the gating on and the phase alignment of the oscillators is measured by counter 1 and counter 2 synchronized by the oscillators clock signals. The measurement result is:

$$T = (n_1 - 1)T_1 - (n_2 - 1)T_2 = (n_1 - n_2)T_1 + (n_2 - 1)r \qquad (2.36)$$

r is the measurement resolution given by T_1-T_2; when $T<T_1$, then $n_1=n_2$ and $T=(n_2-1)r$. In this case a single counter can be used. The resolution of the measurements can be improved using stable oscillators with small difference in frequency. Usually the difference between oscillator frequencies is about 1%, but in some application could be lowered.

A large dynamic range and picoseconds resolution [39,40], can be achieved using the Vernier method. The maximum conversion time is $n_{2max}T_2=T_1T_2/r$.

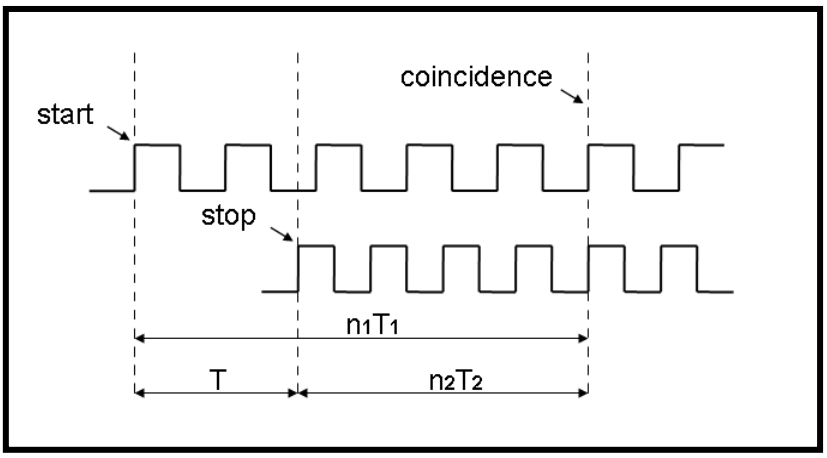


Figure 2.18: Timing diagram of the Vernier method.

2.10 Time-to-digital conversion using digital delay lines

Digital delay lines can be used to measure small time intervals. This method is conceptually simple and is based on the use of the propagation delay of a logic cell as an elementary delay unit. In an ideal case these propagation times are the same for every delay element of the line. The time interval is measured by sampling the state of the line while a pulse propagates through it during the time between the START and STOP instants. The digital delay lines are used in several configuration based on tapped and differential delay lines, the last one is also called Vernier delay line and is realized using two lines of slightly different cell delays. Figure 2.19 (left) shows a tapped delay line created as a train of buffers. In this configuration the state of the delay line is normally at zero level because the START signal is at low level, but when the rising edge of the START signal occurs, it begins propagating through the delay line. Then the rising edge of the STOP signal samples the state of the line, by means of the positive edge triggered flip-flops after each delay unit. The measurements result is determined by the highest position of the flip-flop storing the high level state. The time quantization step of this kind of TDC is determined by the buffer propagation delay τ. The advantage of using this architecture is the very short dead time, furthermore in this way the output from the tapped line is directly digital; a priority encoder can be used to convert the thermometric code into binary natural code.

Figure 2.19 (right) shows a Vernier delay line, it is built by two delay lines; the first is realized by a train of buffers, while the second line is made by transparent latches. Hence the basic delay cell contains one latch having the delay τ_1 and one buffer having the delay τ_2. If the latch delay is longer than the buffer delay, the time quantization step of the TDC is determined by their difference τ_1- τ_2. The time to be measured is defined between the rising edges of the pulses of START and STOP. During the time-to-digital conversion process, the STOP pulse follows the START pulse along the line and all latches from the first cell up to the cell where the START pulse overtakes the STOP pulse are consecutively set. In this approach, the reset input signal is given to all latches simultaneously only after the end of the acquisition time. The two lines working in a differential mode are really close, so in this way, possible non linearity due to temperature and supply variations can be compensated. This technique is able to achieve a good resolution better than the propagation delay of a single logic cell, it resembles the principle of the Vernier oscillators, in fact the delay τ_1 and τ_2 may be regarded as equivalent to the periods T_1 and T_2 of the Vernier method with two oscillators. The drawback of the Vernier delay line is the increased dead time needed in between two different measurements.

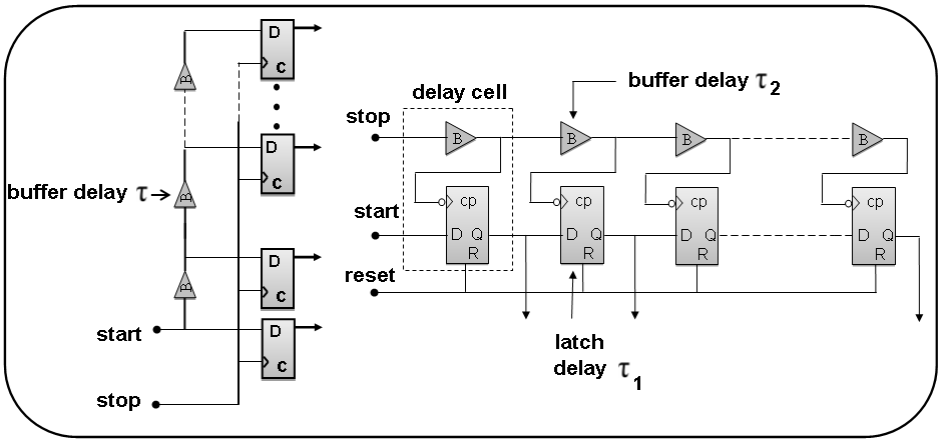


Figure 2.19: Logic block diagram. Left: tapped delay line. Right: Vernier delay line.

In the past years conventional coaxial cables and Printed Circuit Board (PCB) traces were the components of the delay lines used to measure nanosecond time intervals, but with the growth of semiconductor technology new methods have been developed based on digital delay lines implemented in ASIC [41] (Application Specific Integrated Circuit) and FPGA [42] (Field Programmable Gate Array). Rapid progress in FPGA electronics technology allowed achieving a time resolution values in between 10 ps and 500 ps [43,44].

In real delay lines there may be some differences in the propagation times of the delay units and this effect can introduce some non-linearity of the time-to-digital conversion. Furthermore the resolution is also affected by changes of the environment condition, as temperature and power supply. In ASIC devices, the use of an internal PLL (Phase Locked Loop) or DLL (Delay Locked Loop) can provide an automatic stabilization against the changes of these operating parameters.

Chapter 3

TDC architectures

3.1 Introduction

The TDC architectures described in this thesis are based on the Xilinx Virtex-5 Field Programmable Gate Array [45] (FPGA). FPGAs are programmable electronics devices that can reach working frequencies of hundreds of MHz and allow to create complex logic functions and memory elements.

I used the XC5VLX50 with -3 speed grade in order to improve the performance for high-speed design. The approach exploits the classic Nutt method based on multi-stage interpolation. The first stage is built around a coarse 550 MHz free-running counter used to measure long time intervals. The coarse conversion dynamic range is limited to the counter output width. The bin size of the coarse output is limited by the clock period (1.818 ns).

The Virtex-5 Digital Clock Managers (DCMs) provide a wide range of clock management features and allow phase shifting. I used a DCM that gives four copies of the same clock signal shifted by 0° (clk0), 90° (clk90), 180° (clk180) and 270° (clk270). The second stage is built around a state machine synchronized by the DCM output signals, used to perform a first level phase interpolation thus giving a resolution of a quarter of the clock period (about 454 ps). The third stage performs the fine time measurement thus improving the coarse counter resolution. Since I also exploit the four phases information delivered by the DCM, the fine time measurement must only interpolate in between the four different phases i.e. over a quarter of the clock cycle. I designed two different fine time converters in order to compare their performances side by side. The first one consists of tapped delay lines and the second one uses Vernier delay lines.

I used the Xilinx Integrated Software Environment 9.1 (ISE) development tool to realize the different types of TDC architectures [46]; in the design and simulation phase the VHDL (Very high speed integrated circuit Hardware Description Language) [47] has been used.

The main design problem was related to the high frequency design of the coarse TDC and to keep the linearity of the fine TDC output. These problems were solved by manually placing both logic gates and flip-flops.

3.2 Design flow and timing closure approach

The basic elements of a FPGA are the programmable logic blocks and the programmable interconnects. The logic block can perform basic (AND, OR, NOT) or complex logic functions and also includes memory elements. The programmable interconnections allow the logic blocks of a FPGA to be connected as needed by the system designer.

In Virtex-5 FPGA each Configurable Logic Block (CLB) is divided into two slices; each slice consists of 4 flip-flops, 4 6-input Look Up Tables (LUTs) and dedicated carry logic that can be used to cascade function generators in order to implement wide logic functions. These high-speed chain structures are usually used to realize fast counters, adders and multiplexing of data.

Figure 3.1 shows the standard design flow, it comprises the design entry and synthesis, the design implementation and the design verification.

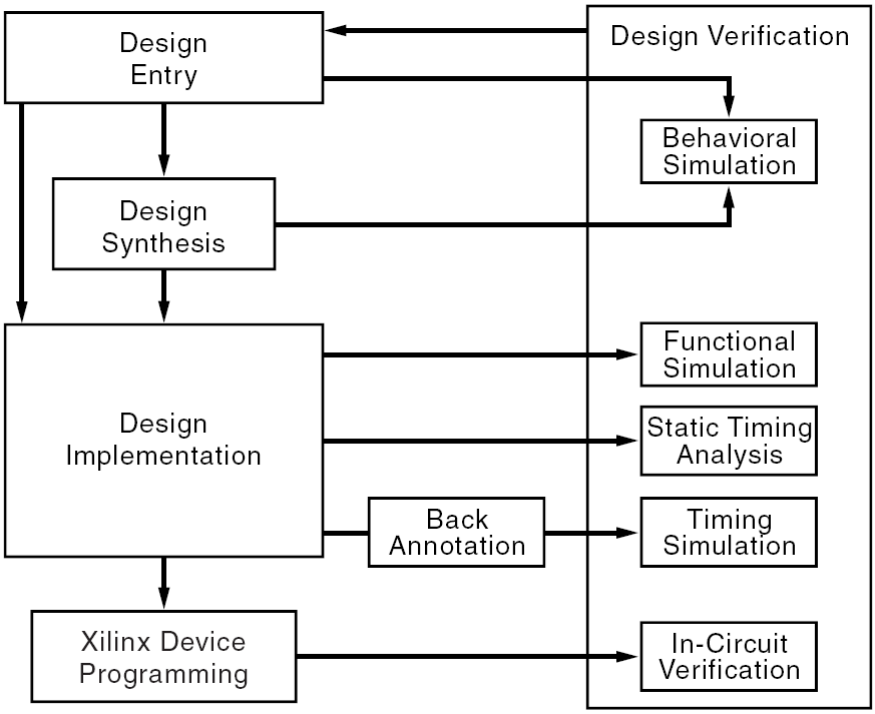


Figure 3.1: Standard design flow.

My design entry is made by VHDL files. These files must be synthesized by the compilation tool into a logical design file format, i.e. a punctual description of the hardware interconnections of logic gates and flip-flops.

The design implementation begins with the mapping or fitting of the logical design file to a specific device and is completed when the physical design is successfully placed and routed and a bitstream file is generated. The propagation delays, inside the programmable device, are calculated during the

implementation procedure. This phase is called back-annotation. The physical design informations are then translated and distributed back to the logical design.

The design verification then tests the functionality and performance of the implemented logic. This task is accomplished by making the functional and timing simulations, the static timing analysis and finally the in-circuit verification. The design verification procedures take place throughout the design process. Functional simulation determines if the logic in the design is correct before implementing it in the device. Timing simulation verifies that the implementation runs at the desired speed under worst-case conditions. Static timing analysis is used for quick timing checks of a design after it is placed and routed. It also allows to determine path delays in the design. The final test of the design consists of performance measurement in the target application. In-circuit verification tests the circuit under typical operating conditions. Different iterations of the design can be loaded into the device and test it in-circuit because the device is reprogrammable.

The high speed design puts several constraints on the mapping, the placement and routing of the logic. There can be only one level of logic gate between the output and the input of several flip-flops. Logic functions that need several inputs, normally using more than one logic level, had to be pipelined between more clock cycles. This strategy increases performance at the expense of adding latency. Depending on the application, the dedicated slice carry logic can be used to provide wider logic functions.

Some flip-flops input have to be driven by logic elements inside the same slice of the Virtex-5 FPGA in order to lower the number of routing nets on the signal combinatorial paths. Figure 3.2 shows the simplified circuit block diagram of this timing closure approach; some elements of the Virtex-5 FPGA slice are omitted for clarity. The flip-flops in the slices are configured as positive edge triggered D-type.

The source flip-flops FFA and FFD are located in the slice A; they drive a LUT (Look Up Table, 6 input function generator) packed with another flip-flop FFD in a surrounding slice. The LUT is configured in order to realize a 2 inputs combinatorial function (as AND, OR, etc..). Several routing connections between the two slices are possible and the Xilinx ISE software finds the most optimal routes. All of the interconnect features are transparent to the FPGA designers that can view the delay of these nets using FPGA Editor. In order to verify the tight timing requirement of a high speed design, the routing connections Net A and Net B have to be as short as possible and with fewer hops; in fact the propagation delay of these nets have to be lower than 1 ns. The value of the maximum propagation delay of these nets is related to the slice timing parameter and is calculated in order to avoid a metastability problem of the flip-flops therein the slice.

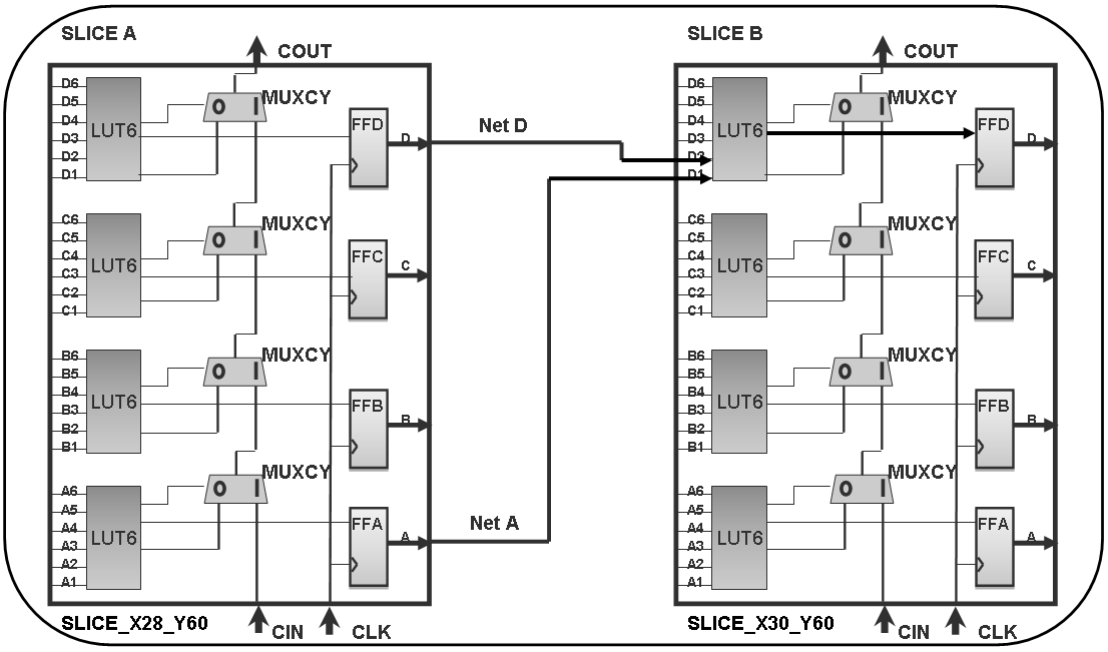


Figure 3.2: Simplified circuit block diagram of the timing closure approach.

Metastability could happen when a data is changing at the instant of the clock signal rising edge. The result is that the output may behave unpredictably, taking more time than normal to settle to its correct state, or even oscillating several times before settling. It can be avoided by ensuring that the data inputs are held valid and constant for specified periods before and after the clock signal rising edge, called the set up time (T_{su}) and the hold time (T_h) respectively. Another relevant timing value for this analysis is the flip-flop clock to output delay, which is the time the flip-flop takes to change its output after the clock edge (T_{cko}). Figure 3.3 shows the timing characteristic of a positive edge triggered D-type flip-flop.

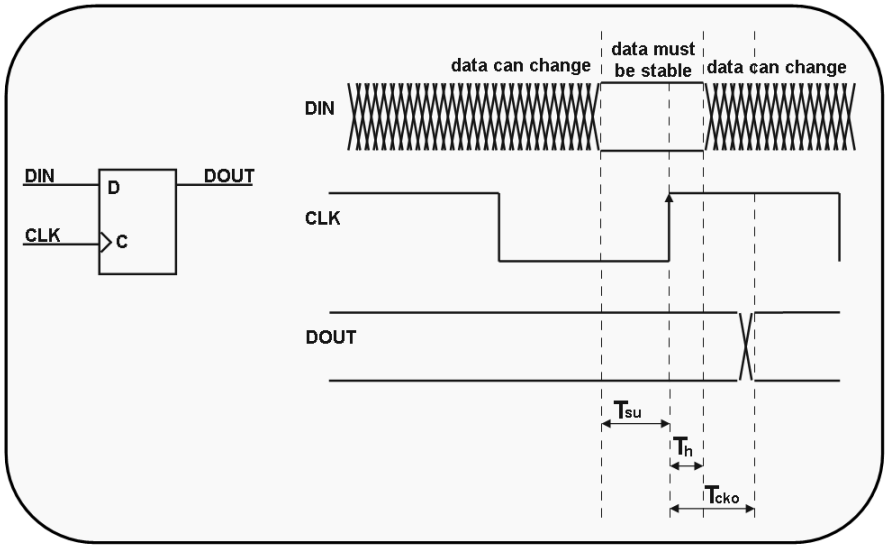


Figure 3.3: Flip-flop timing characteristics.

Table 3.1 shows the slice timing parameters of the Xilinx Virtex-5 FPGA with -3 speed grade, these specification are representative of worst-case supply voltage and junction temperature conditions. The value of T_{cko} reported in table 3.1 is the maximum clock to output propagation time.

T_{su}	0.36 ns	Time before the clock that data from the AX/BX/CX/DX inputs of the slice must be stable at the D input of the slice flip-flop
T_h	0.19 ns	Time after the clock that data from the AX/BX/CX/DX inputs of the slice must be stable at the D input of the slice flip-flop
T_{cko}	0.35 ns	Time after the clock that data is stable at the outputs of the slice flip-flops FFA/FFB/FFC/FFD

Table 3.1: Slice timing parameter value.

The LUT introduces a propagation delay from the inputs D1/D2 of the slice to the input of the flip-flop FFD located into the slice B, but it is taken in account in the FFD set up and hold times; in fact they are calculated at the D1/D2 slice inputs. The signals driven by the LUT can exit the slice bypassing the flip-flop, in that case the propagation delay from the input to the output of the slice is 0.08 ns.

The maximum frequency f_0 of the circuit shown in figure 3.2 can be computed as a function of the clock to output time T_{cko} of the flip-flop FFA and FFD located into the slice A, of the propagation time T_{net} of the longest one between Net A and the Net D, of the set up time T_{su} of the flip-flop FFD located into the slice B and to the possible skew T_{skew} of the clock signal synchronizing the slice A and slice B via the following formula:

$$f_0 = 1/T_0 = 1/(T_{cko} + T_{su} + T_{net} + T_{skew}) \qquad (3.1)$$

Using the values of Table 3.1:

$$f_0 = 1/T_0 = 1/(0.35\ ns + 0.36\ ns + T_{net} + T_{skew}) = 1/(0.71\ ns + T_{net} + T_{skew}) \quad (3.2)$$

The clock system frequency used is 550 MHz and the clock period is 1.818 ns. In order to avoid set up time violations, the sum of the maximum propagation time of the nets and the time skew between the source and receiving slices have to be lower than 1.108 ns (1.818 ns – 0.71 ns).

A good design approach is to place the driving and the receiving slices very close, which means that the routing delays had to be lower than 1 ns. The short distance between slices also implies lower skew values of the clock signal, so that the sum of T_{net} and T_{skew} will be at most 1.108 ns.

In this fashion, no set up time violations are allowed. The hold time is assured by the following relation:

$$T_h < T_{cko} + T_{net} + T_{skew} \quad => \quad T_{cko} + T_{net} + T_{skew} > 0.19\ ns \qquad (3.\ 3)$$

Static timing analysis allows to determine path delays of the design and together with several simulations allows to detect set up time and hold time violations.

3.3 TDC architecture

Figure 3.4 shows the simplified circuit block diagram of the TDC architecture. The external clock frequency is 550 MHz. Figure 3.5 shows the Virtex-5 DCM clock signal shifting operation. The clk0, clk90, clk180, clk270 outputs are each phase-shifted by ¼ of the input clock period T_0 relative to each other. So, the period T_0 can be split in four quarters using the rising edges of the four phases of the clock signal.

The coarse TDC is built around the counter and the state machine. It cannot process the hit signals immediately, because the sampling time could take place while the async_start and async_stop signals could not be stable. Therefore signals are first synchronized and then they are processed by the coarse TDC.

The building blocks of the TDC are the synchronizer, the coarse TDC and the fine TDCs.

I designed two TDC architectures in which the fine TDC is achieved with two different methods. The first one consists of tapped delay lines, the second one uses Vernier delay lines.

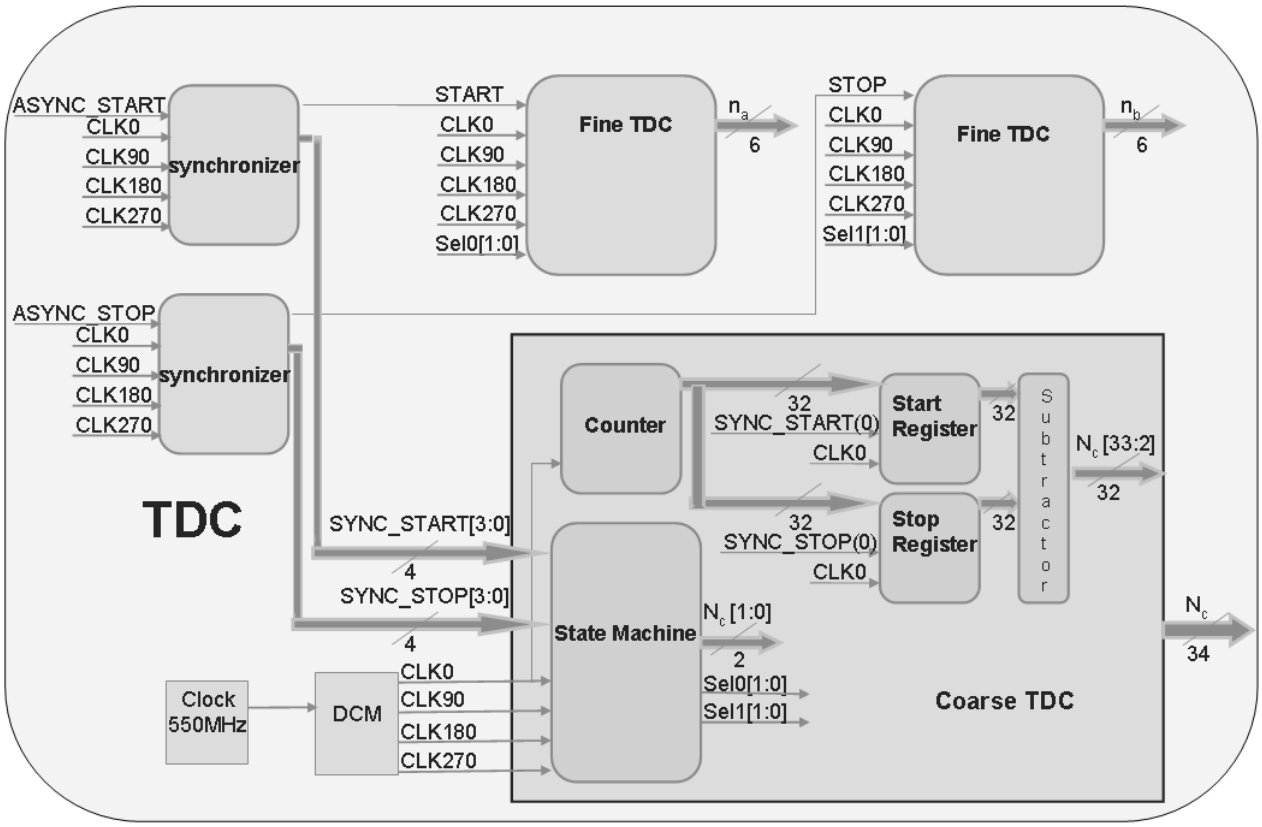


Figure 3.4: Simplified circuit block diagram of the TDC architecture.

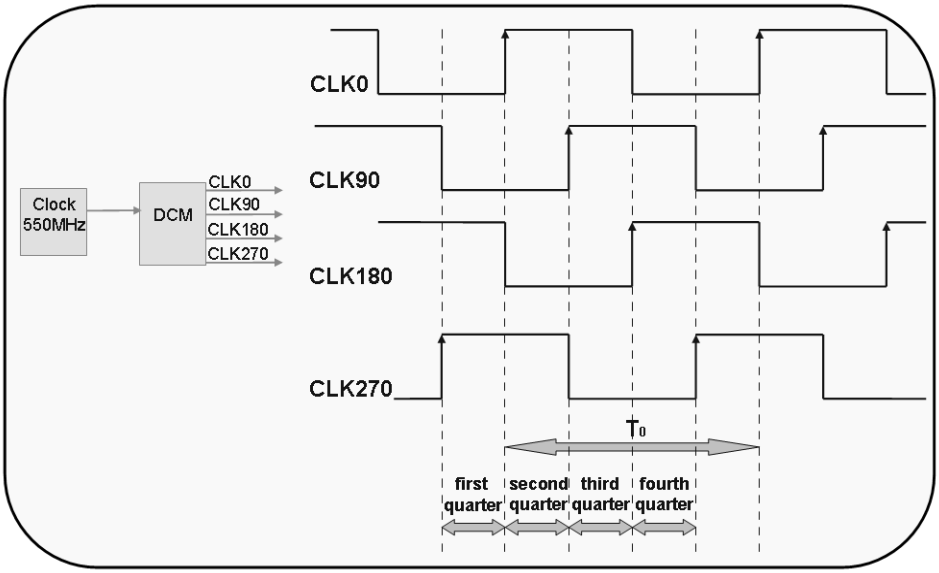


Figure 3.5: Virtex-5 DCM clock signal shifting operation.

3.3.1 The synchronizer

Figure 3.6 shows the block diagram of the synchronizer, it is used to synchronize the async_start and async_stop signals to the clock signals clk0, clk90, clk180, clk270. It is built by four synchronizer stages, the stage 0 performs the synchronization of the async_start or async_stop signal to the clock clk0, stage 1 to clk90, stage 2 to clk180 and stage 3 to clk270. The output of the synchronizer is made by four signals sync_start[3:0]/sync_stop[3:0], synchronous to the four phases of the clock system, delivering to the coarse TDC and by a start/stop signal delivering to the fine TDC. The propagating delays of the asynchronous signal through the synchronizing stages can be different, due to the routing in the FPGA device. The resulting skew of the async_start or async_stop signal can bias the measurements.

Figure 3.7 shows the circuit block diagram of the synchronizer stage. The flip-flop FF0 is used to detect a rising edge of the asynchronous input signal. The output of FF0 is then sampled by four flip-flops FF1, FF2, FF3, FF4. They are placed in the same slice; in this way a negligible skew, ideally zero, of the clock signal CLOCK is achieved. So in order to reduce the metastability of these four flip-flops, which could happen if their input in not held valid and constant for the specified set up time (T_{su}) and hold time (T_h), the FF3 and FF4 input are delayed ad hoc. Furthermore the routing of the FF0 output net assures slightly different propagations times to the flip-flops inputs. The metastability window is given by the sum of T_{su} and T_h and is equal to 0.55 ns. This value is representative of worst-case supply voltage and junction temperature conditions. The subsequent OR4 gate ensures that one flip-flop output is at high logic level and that the flip-flop FF5 sampling

OR4_OUT (the gate AND3B2 is transparent in this case because the other two inputs are at zero level) is used to further reduce the possible metastability of the previous stage.

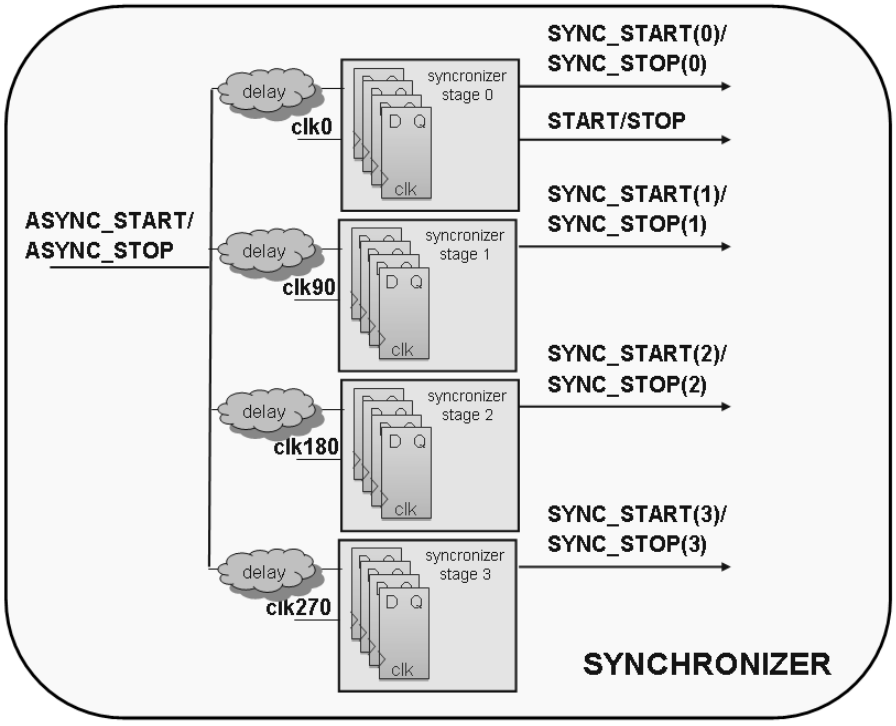


Figure 3.6: Simplified block diagram of the synchronizer.

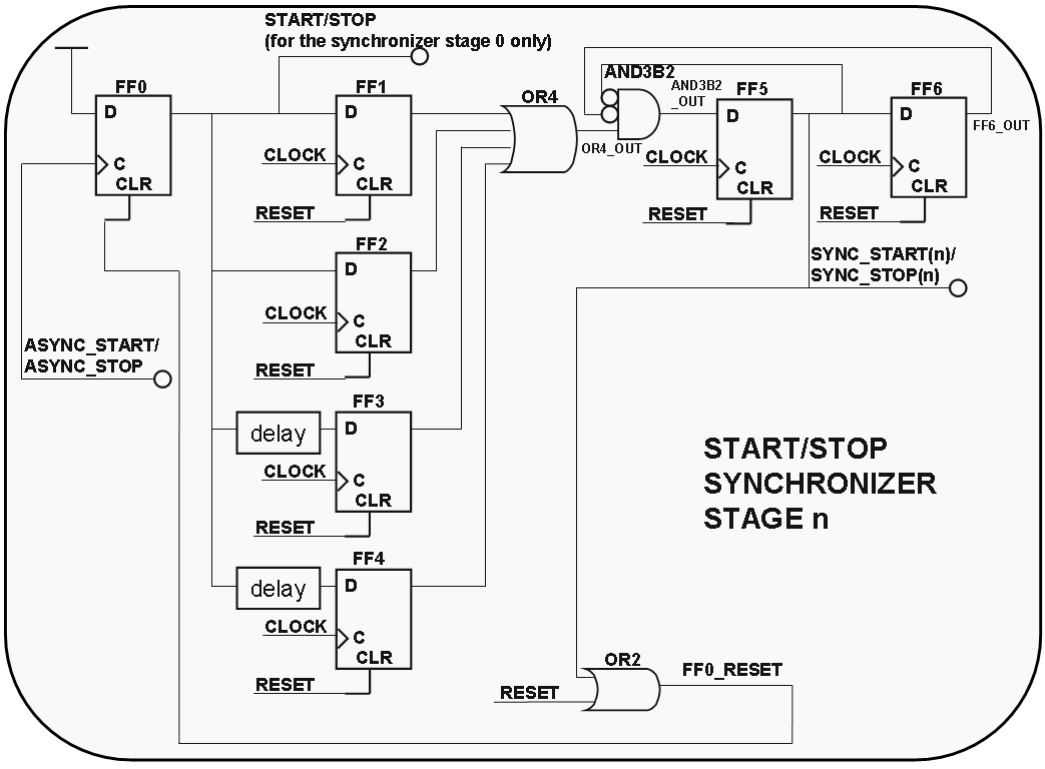


Figure 3.7: Circuit block diagram of the synchronizer stage.

The feedback path given by the FF5 output guarantees that the FF5 output is at high level for just one clock period. Therefore the sync_start(n)/sync_stop(n) signal will be at the high level for one clock period after a clock cycle from the detection of the rising edge of the async_start/async_stop signal. The sync_start(n)/sync_stop(n) drives also the OR2 gate used to reset the FF0 flip-flop. The FF6 flip-flop function will be clear after a timing propagation analysis of the synchronizer stage. Figure 3.8 shows the waveforms of the synchronizing operation.

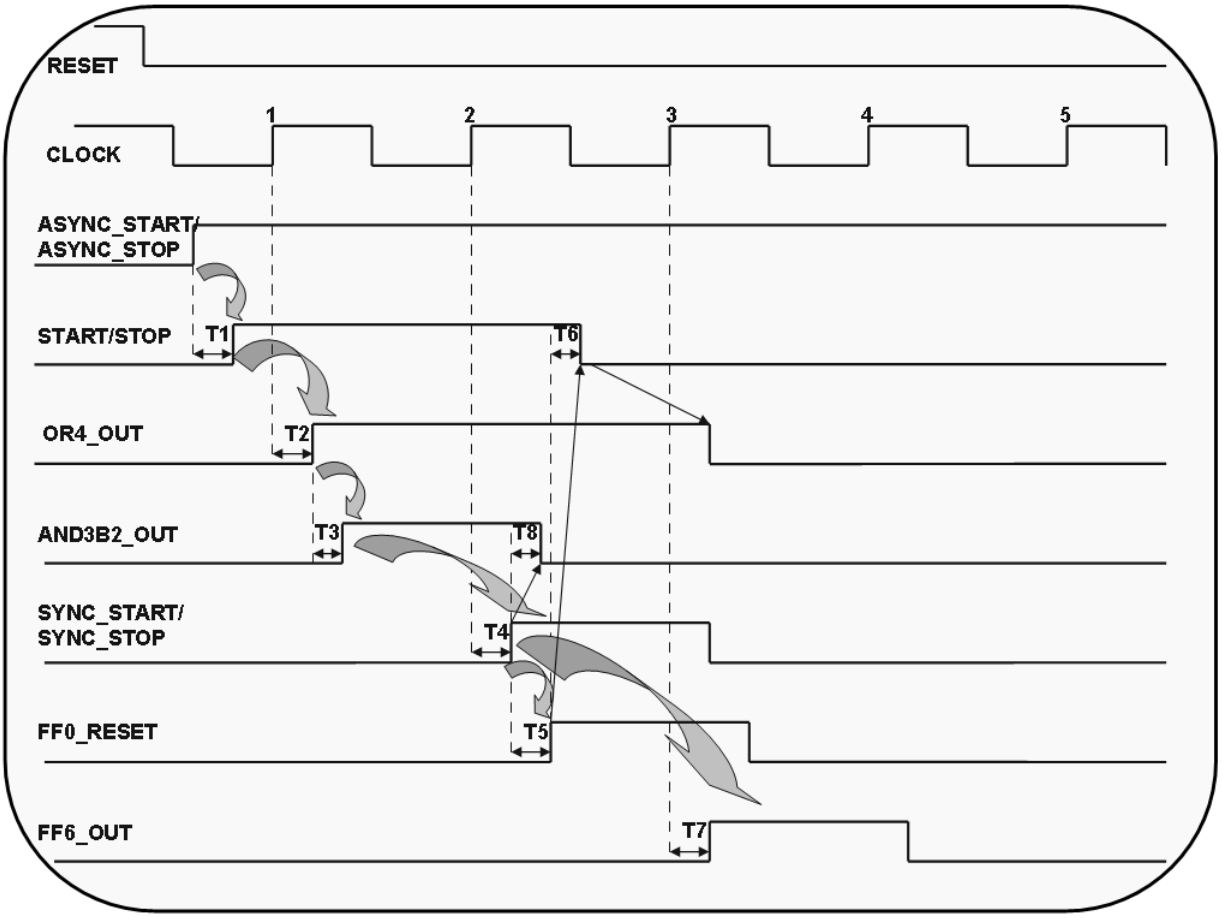


Figure 3.8: Waveforms of the synchronizing operation (1).

The time T1 is the sum of T_{cko} of FF0 and the shortest time between the propagation times of the net start/stop driving FF1, FF2, FF3, FF4 inputs.

The time T2 is the sum of the shortest time between the (T_{cko} + T_{net}) of FF1, FF2, FF3, FF4 outputs and the OR4 gate propagation time.

The time T3 is the propagation time of the AND3B2 gate.

Using the timing closure approach of figure 3.1, the OR4 gate and the AND3B2 will be mapped in the same LUT6. It implies a shortening of their propagation time.

The time T4 is the T_{cko} of FF5.

The time T5 is the sum of the propagation time of the OR2 gate (LUT configured as OR2) and the propagation time of the net sync_start(n)/sync_stop(n) from the FF5 output to the OR2 input.

The time T6 is the sum of the propagation time of the net FF0_reset and the clear to output time T_{clr} of FF0 (the propagation delay for an asynchronous reset of the flip-flop from the CLR input to the output; 0.74 ns) and the longest between the propagation times of the net start/stop driving FF1, FF2, FF3, FF4 inputs.

The time T7 is the T_{cko} of FF6.

The time T8 is the sum of the propagation time of the AND3B2 gate and the propagation time of the net sync_start(n)/sync_stop(n) from the FF5 output to the AND3B2 input.

Figure 3.9 shows the waveforms of the synchronizing operation when the following relationship is not satisfied. T_0 is the clock system period, T_{su} is the set up time of the flip-flop (between FF1, FF2, FF3, FF4) driven by the longest start/stop net:

$$T4 + T5 + T6 < T_0 - T_{su} \quad (3.4)$$

The relationship (3.4) can be written as:

$$T_{cko} + T_{FF5toOR2} + T_{LUT} + T_{OR2toFF0} + T_{clr} + T_{FF0toFF(1/2/3/4)} + T_{su} < T_0 \quad (3.5)$$

$$T_{FF5toOR2} + T_{OR2toFF0} + T_{FF0toFF(1/2/3/4)} < 1.818\ ns - (0.35\ ns + 0.08\ ns + 0.74\ ns + 0.36\ ns) \quad (3.6)$$

$$T_{FF5toOR2} + T_{OR2toFF0} + T_{FF0toFF(1/2/3/4)} < 0.288\ ns \quad (3.7)$$

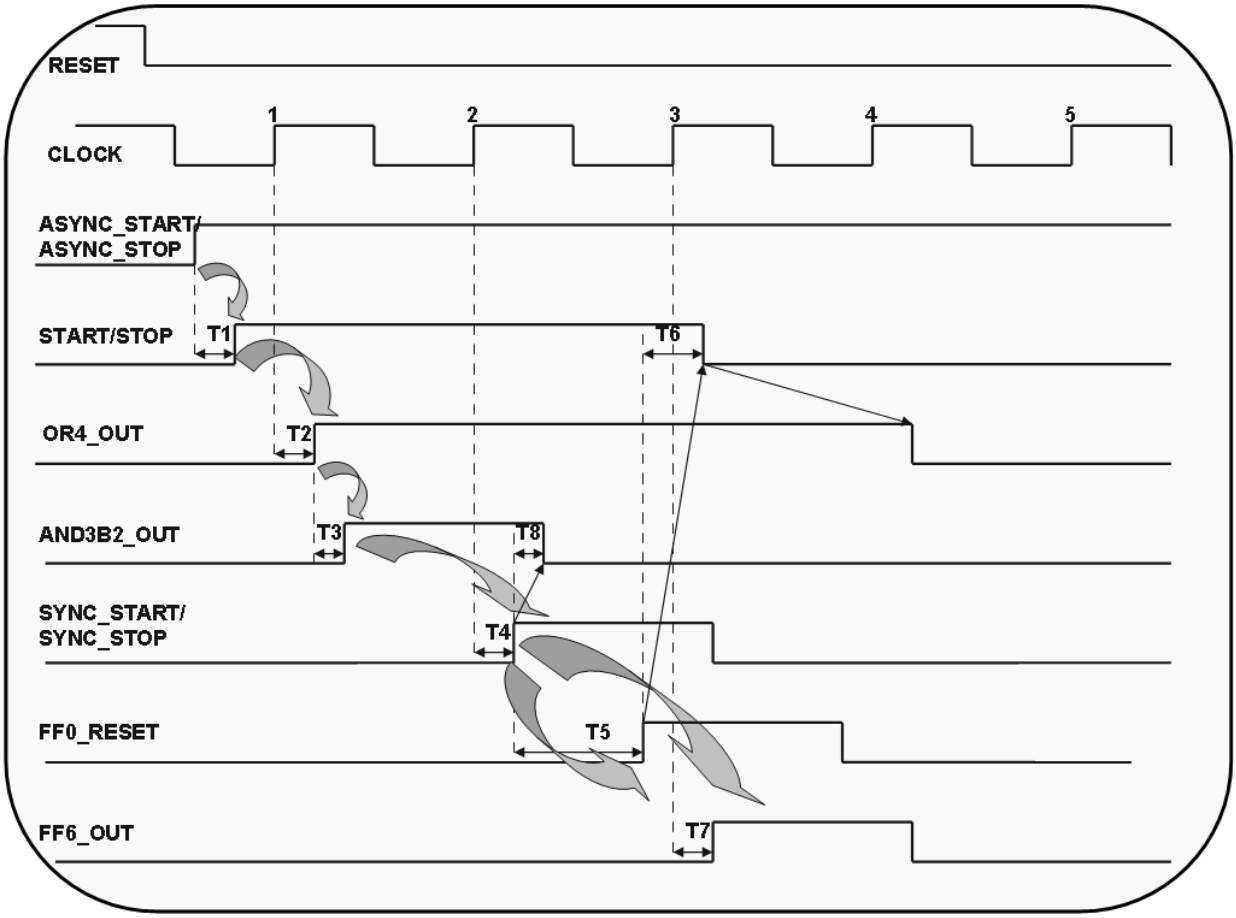


Figure 3.9: Waveforms of the synchronizing operation (2).

In the example shown the relationship (3.7) is not satisfied, in fact the sum of the propagation time of three routing nets is higher than 0.288 ns. Therefore it's mandatory to set (by means of the FF6_out) the AND3B2_out to a low level during the third clock cycle of figure 3.9. In fact without the flip-flop FF6, the flip-flop FF5 would sample again a high level on the fourth clock signal rising edge delivering two pulses, instead of one. Figure 3.10 shows the waveforms of the synchronizing operation of the circuit without the flip-flop FF6.

Figure 3.11 shows the waveform of the synchronizer outputs.

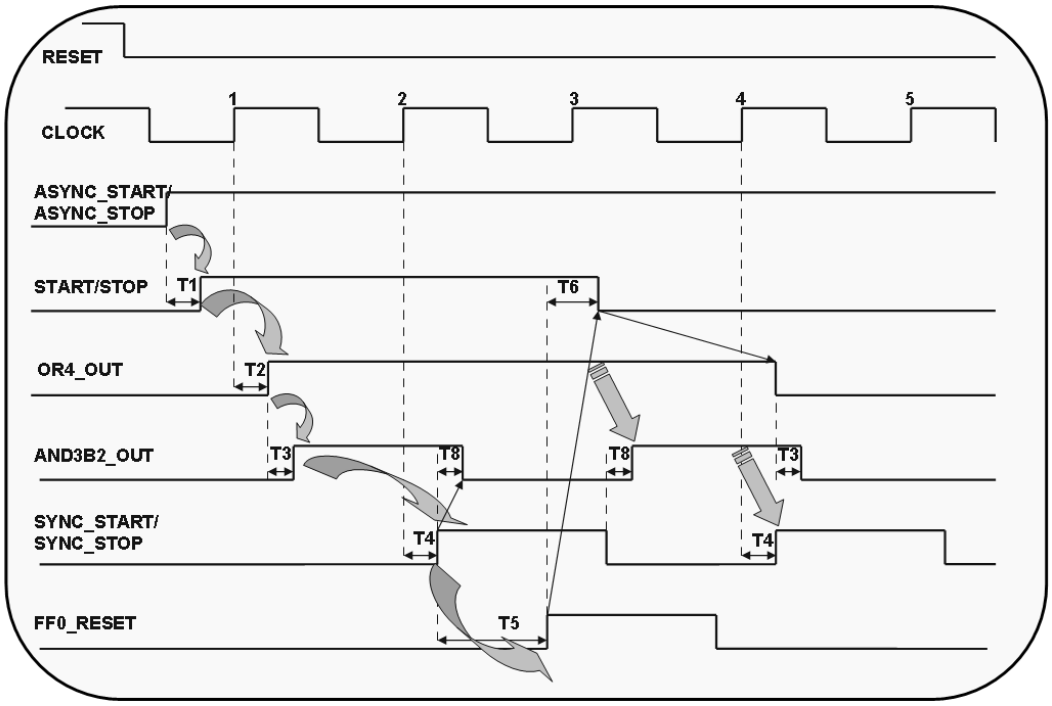


Figure 3.10: Waveforms of the synchronizing operation (3).

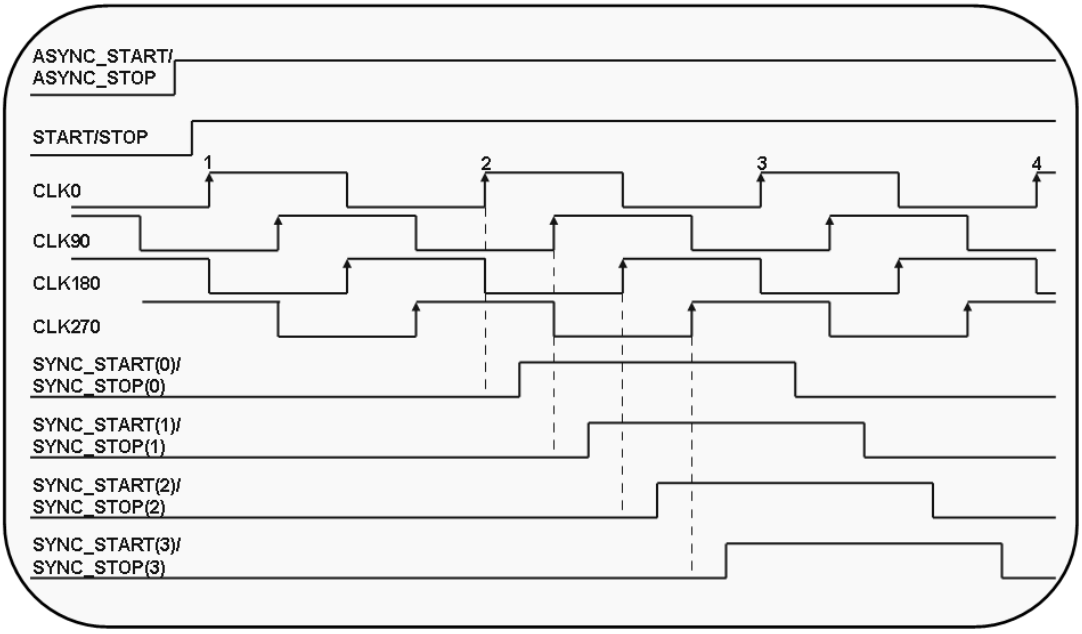


Figure 3.11: Waveforms of the synchronizer outputs.

3.3.2 The coarse TDC

The building blocks of the coarse TDC are the 550 MHz synchronous binary counter and the finite state machine. The coarse counter has a 32 bit data width and is used in free-running mode. This counter is reset only at power up. When the start signal transitions occurs, the synchronizer drives a pulse of one clock period width on the sync_start(0) line and then the current state of the counter is sampled by the start register. The same operation occurs also when the stop signal is delivered to the TDC; in this case the synchronizer drives a pulse of one clock period width on the sync_stop(0) line and then the current state of the counter is sampled by the stop register. The difference between the stop and the start register is the coarse measurement of the time interval.

The task of the finite state machine, shown in Figure 3.12, is to perform a first phase interpolation thus improving the time resolution of the coarse counter to a quarter of the clock period. Furthermore it is also used to select the proper delay line of the fine TDC performed in the carry chain and Vernier delay lines architectures.

The state machine is built around the state counter, it changes the output value every quarter of the clock period.

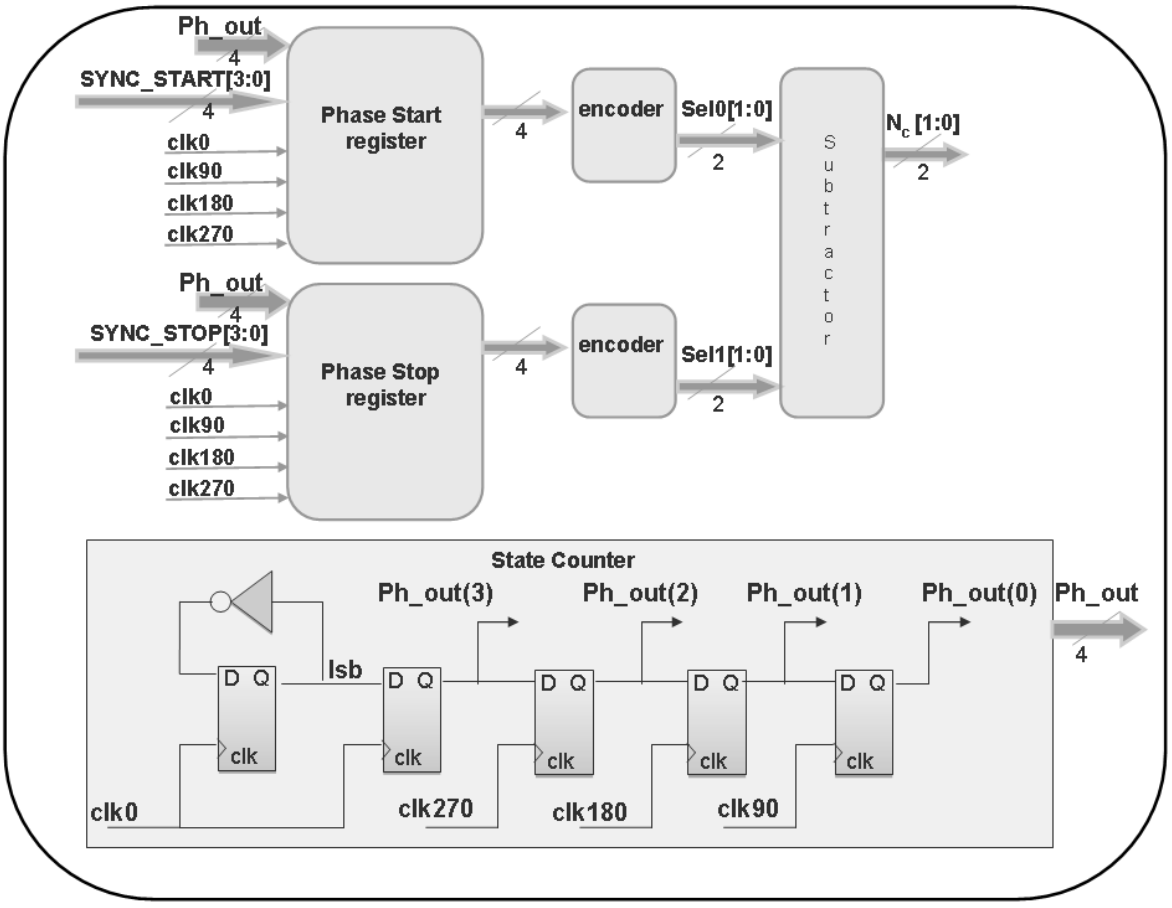


Figure 3.12: Simplified block diagram of the finite state machine.

The lsb signal of the state counter, shown in figure 3.12, is the least significant bit of the 32 bit width free running counter shown in figure 3.4. Tables 3.2 shows the state counter outputs.

Ph_out(3)	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Ph_out(2)	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1
Ph_out(1)	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Ph_out(0)	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
Decimal output	5	4	6	2	10	11	9	13	5	4	6	2	10	11	9	13	5	4	6	2	10	11	9	13
Decoded decimal output	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1

Table 3.2: State counter outputs.

When the start signal transition occurs, the synchronizer drives a pulse of one clock period width on the sync_start[3:0] lines and then the current state of the counter is sampled by the phase start register. The same operation occurs also when the stop signal is delivered to the TDC; in this case the synchronizer drives a pulse of one clock period width on the sync_stop[3:0] lines and then the current state of the counter is sampled by the phase stop register. Figure 3.13 shows the phase start/stop register. Figures 3.14 and 3.15 show the waveforms of the sampling of the state counter outputs by means of the phase start/stop register. If the rising edge of the start/stop signal is within the first quarter of the clock period the output of the phase start/stop register could be “1101” (or “0010”), as shown in figure 3.14. If the rising edge of the start/stop signal is in the subsequent quarter of the clock period the output of the phase start/stop register is the next value of the state counter, then it is “0101” (or “1010” if the previous output was “0010”), as shown in figure 3.15.

When the start and stop signal transitions occur (with a latency of two clock cycles due to the synchronizer) the phase difference between the start and stop rising edges is detected. The start and the stop registers sample the state counter outputs. The least significant bit corresponds to a quarter of the clock period. The 2 bit subtractor output N_c[1:0] encodes the value of the phase difference.

The sel0/1[1:0] outputs, shown in Figure 3.12, follow the phase difference between the start/stop and the clk0 signal. This value is “00” if the phase difference is between $3\pi/2$ and 0, “01” if it is between 0 and $\pi/2$, “10” if it is between $\pi/2$ and π, and “11” if it is between π and $3\pi/2$.

The coarse TDC output word is formed as a 34 bit word since it consists of the 32 bit counter word and the 2 bit N_c[1:0] added bits.

The LSB state machine counter value is 454 ps.

The fine TDC therefore is only used to interpolate the phase in one quarter of the clock period. In the delay line TDC architecture the selection of the delay line of the fine time measurements reflects

the phase difference between the start/stop signal and clk0. The measurement range of the coarse TDC is limited by the counter width and the resolution is limited by the clock frequency.

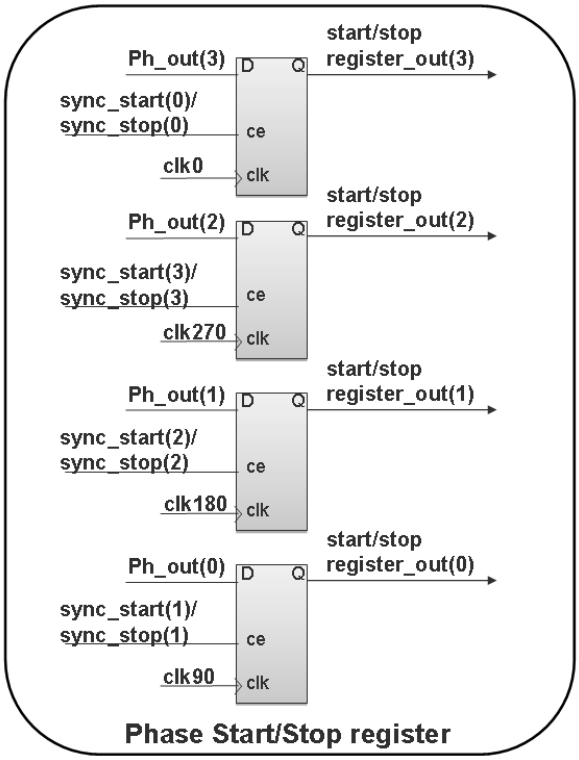


Figure 3.13: Phase start/stop register.

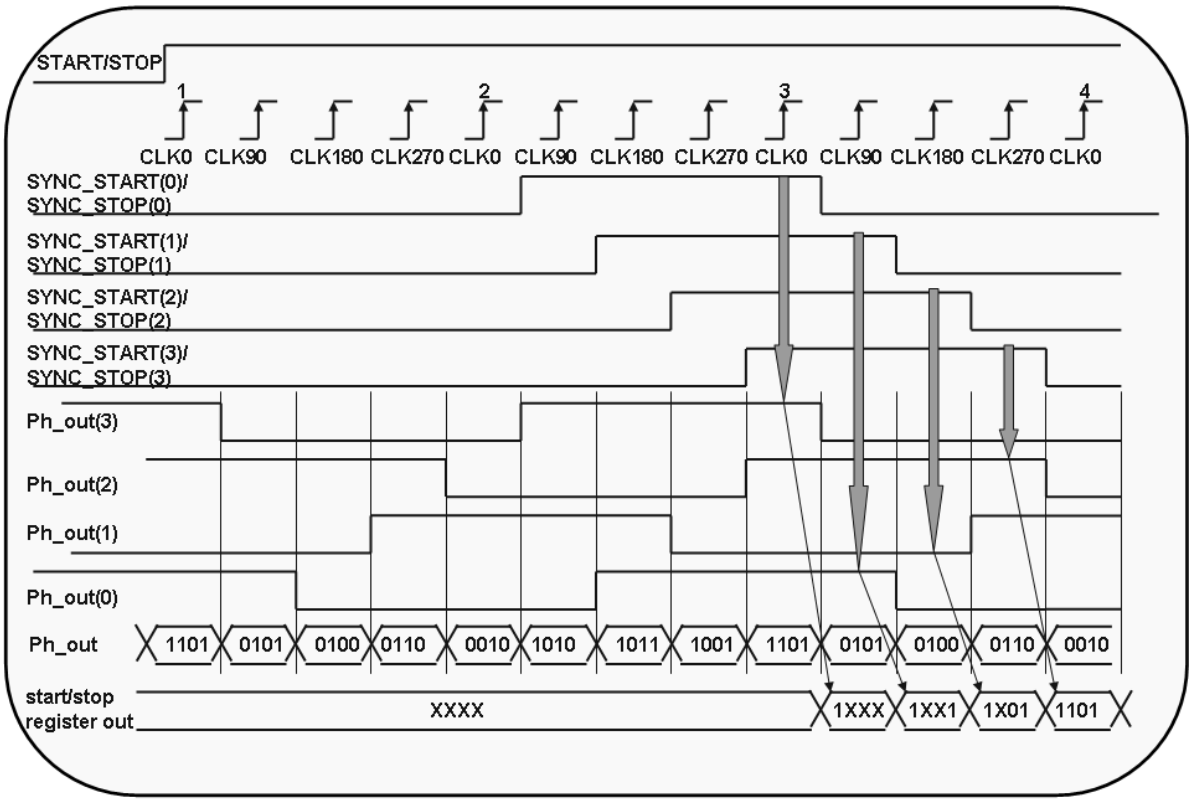


Figure 3.14: Waveforms of the sampling of the state counter output(1).

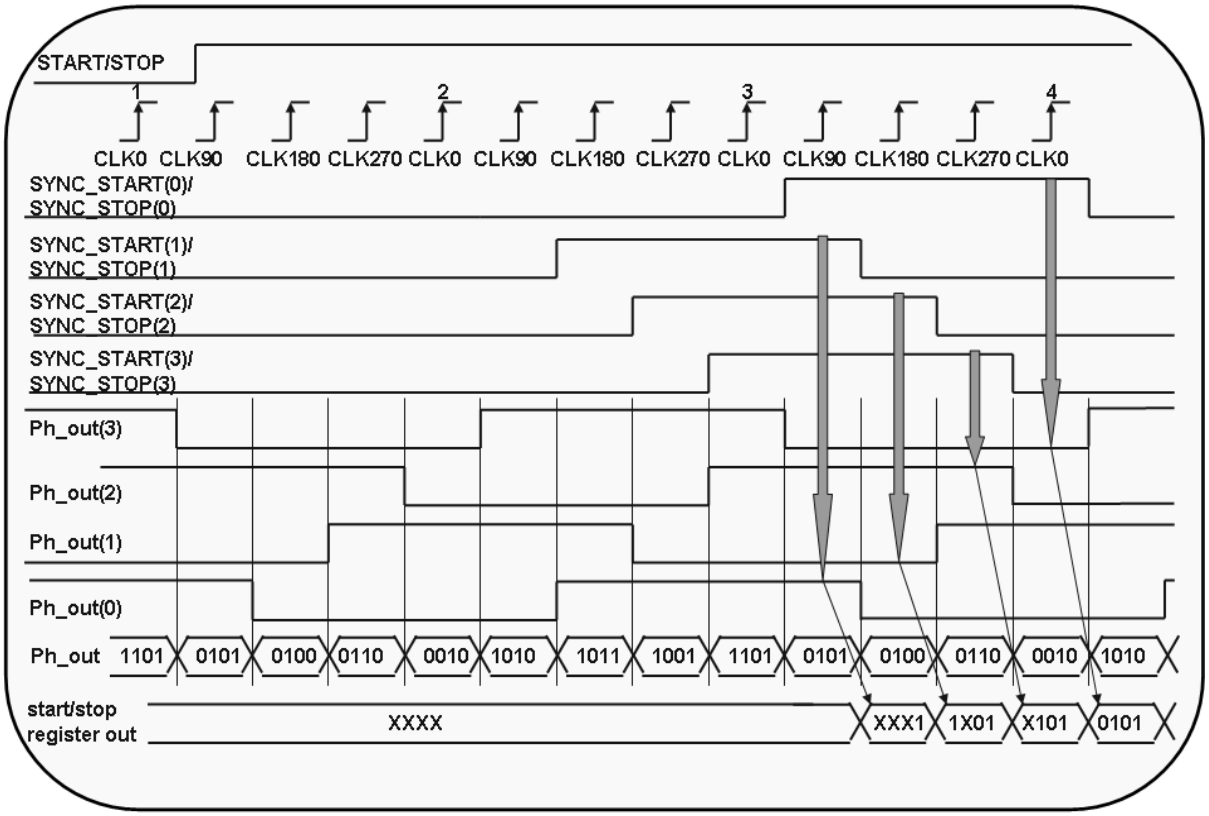


Figure 3.15: Waveforms of the sampling of the state counter output(2).

3.3.3 Carry chain delay line

The carry chain delay line is shown in Figure 3.16. I have used high-speed chain structures that vendors designed for general-purpose applications. In this configuration the stop signal is the 550 MHz system clock. The start signal after each delay unit is sampled by the corresponding flip-flop on the rising edge of the stop signal. In this configuration the delay line consists of set of 64 multiplexers in sequence.

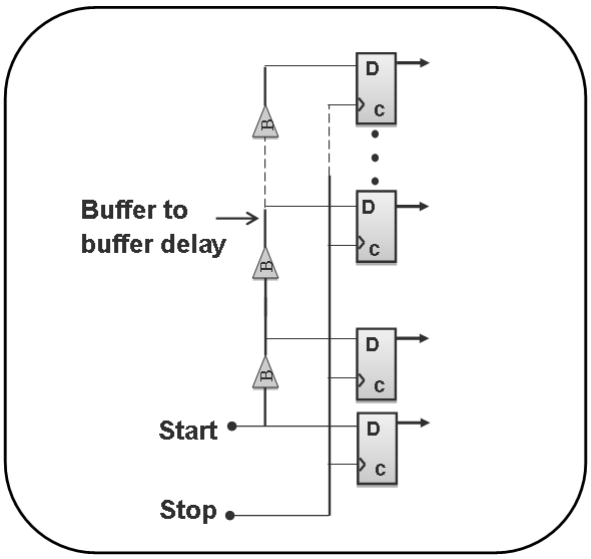


Figure 3.16: Carry chain delay line.

The selection bit of every multiplexer is set to logic value one, in order to let the start signal propagate through the line. The time quantization step of the TDC is determined by the multiplexer propagation delay time τ. Due to the short delay of the tapped delay line, it's necessary to use four delay lines in order to cover the full clock period. The four lines are clocked by the clk0, clk90, clk180, clk270 signals delivered by the DCM. The value of the delay lines is stored in four registers and then the state machine selects the right delay line by asserting the sel0/1[1:0] bits.

In Figure 3.17 a simplified block diagram of the Virtex-5 slice is shown. The carry chain delay lines are implemented in a small region of the device and every line uses 8 slices of it. I decided to use four delay lines rather than a longer one, to reduce the possible non linearity introduced by the clock distribution between neighbouring slices. Furthermore in this way, the output from the tapped line is converted from thermometric code into binary natural code by using a priority encoder. A very short dead time (about 1 clock period) is the main advantage of using carry chain delay line.

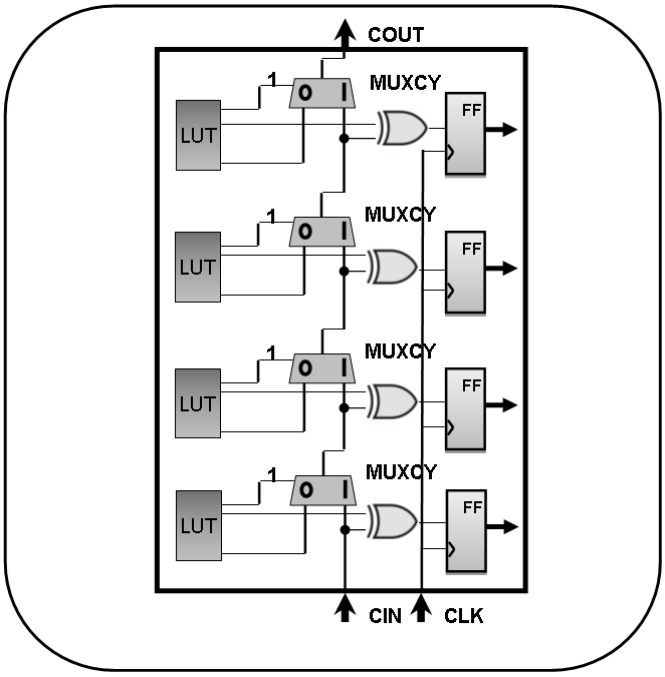


Figure 3.17: Simplified circuit block diagram of the Virtex-5 slice.

3.3.4 Vernier delay line

The second fine TDC architecture, shown in Figure 3.18 consists of two tapped rows working in differential mode. The first is created as a chain of 64 latch flip-flops and the other as a chain of 64 non inverting buffers. Hence the basic delay cell contains one latch having the delay τ_1 and one buffer having the delay τ_2. If the latch delay is longer than the buffer one, the time quantization step of the TDC is determined by their difference τ_1- τ_2. The time to be measured is defined between the rising edges of the pulses start and stop. During the time-to-digital conversion process, the stop pulse follows the start pulse along the line and all latches from the first cell up to the cell where the

start pulse overtakes the stop pulse are consecutively set. In this approach, the reset input signal is given to all latches contemporaneous only after the end of the acquisition time.

As in the carry chain architecture, it's necessary to use four delay lines in order to cover the full clock period. The stop signal is generated by clk0, clk90, clk180, and clk270 in the 4 different delay lines. The start and stop signals have to be stable during the propagation along the lines. Thus their level is kept constant until the end of the acquisition time. The differential lines are implemented in 64 slices of the device. The two lines working in a differential mode are really close, in this way possible non linearity induced by temperature and power supply variations can be compensated. The drawback of the Vernier delay line is the increased dead time needed in between two different measurements.

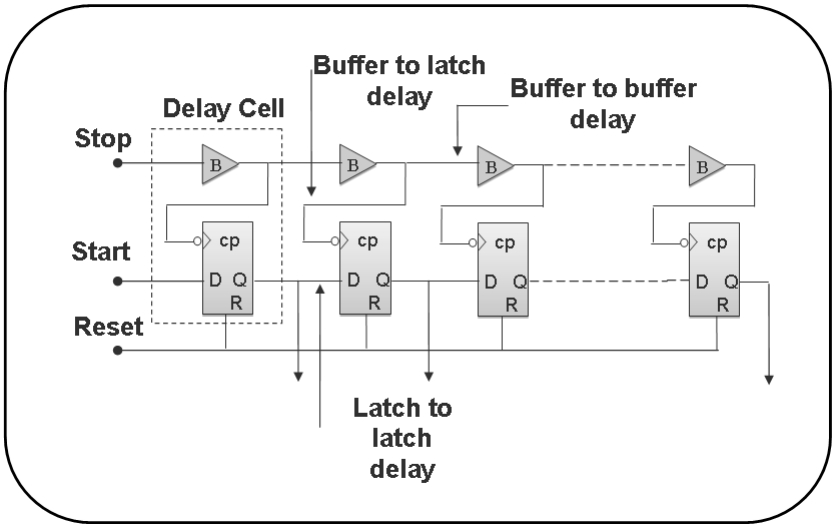


Figure 3.18: Vernier delay line.

3.4 FPGA implementation of the TDC architectures

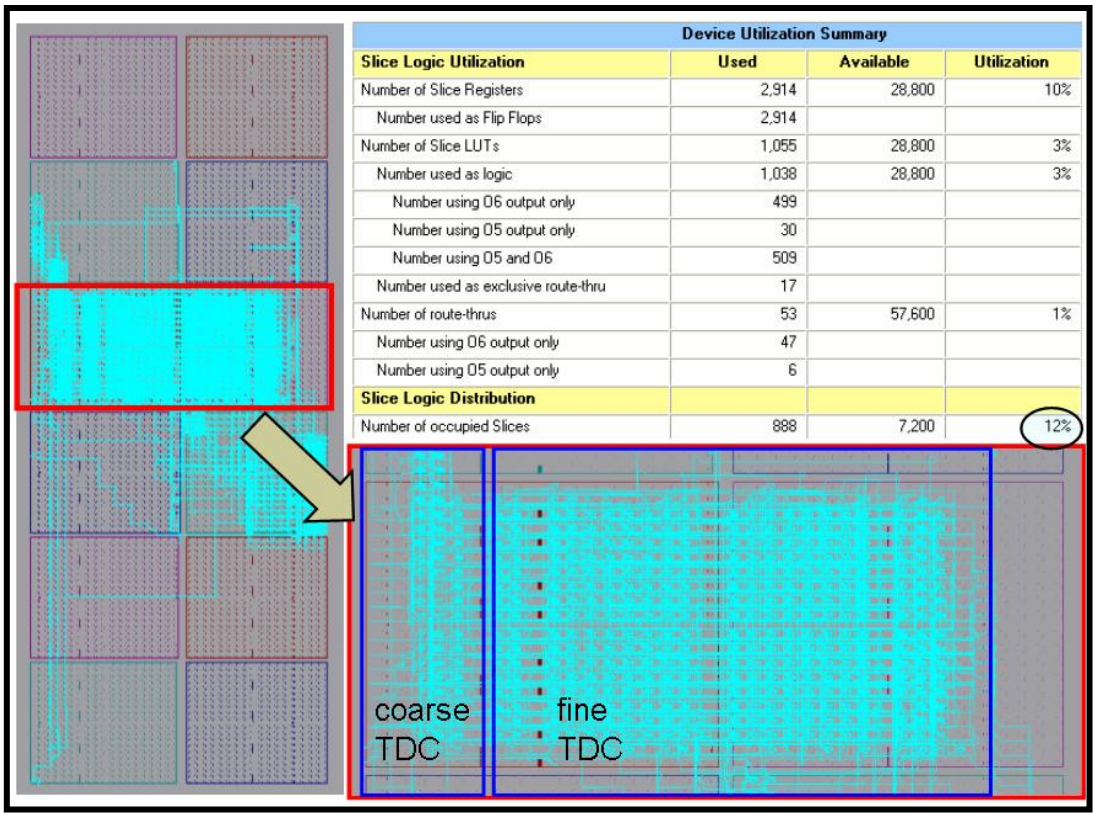
The TDC architectures are implemented in the Xilinx Virtex-5 FPGA. They have different device occupancies.

Figure 3.19 shows the carry chain delay line TDC implementation.

It should be noted that the occupancy of this kind of TDC is about two clock regions of the device and the number of occupied slices is about 12%. This number accounts also the read out electronic placed outside the red line border.

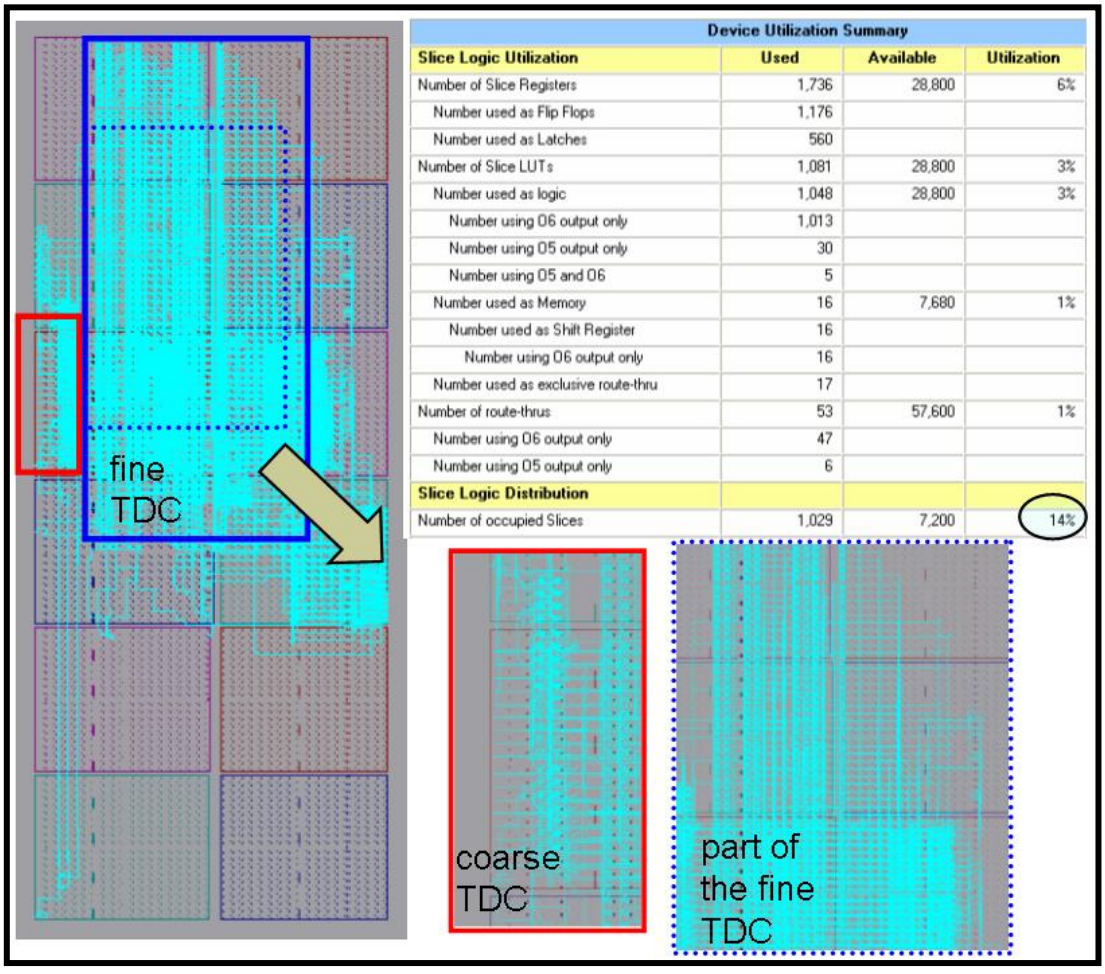
Figure 3.20 shows the Vernier delay line TDC implementation.

In this case the occupancy of the delay lines is beyond two clock regions. The number of occupied slices is 14%, that is about the same of the carry chain delay line architecture.



Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	2,914	28,800	10%
Number used as Flip Flops	2,914		
Number of Slice LUTs	1,055	28,800	3%
Number used as logic	1,038	28,800	3%
Number using O6 output only	499		
Number using O5 output only	30		
Number using O5 and O6	509		
Number used as exclusive route-thru	17		
Number of route-thrus	53	57,600	1%
Number using O6 output only	47		
Number using O5 output only	6		
Slice Logic Distribution			
Number of occupied Slices	888	7,200	12%

Figure 3.19: Carry chain delay line TDC implementation.



Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1,736	28,800	6%
Number used as Flip Flops	1,176		
Number used as Latches	560		
Number of Slice LUTs	1,081	28,800	3%
Number used as logic	1,048	28,800	3%
Number using O6 output only	1,013		
Number using O5 output only	30		
Number using O5 and O6	5		
Number used as Memory	16	7,680	1%
Number used as Shift Register	16		
Number using O6 output only	16		
Number used as exclusive route-thru	17		
Number of route-thrus	53	57,600	1%
Number using O6 output only	47		
Number using O5 output only	6		
Slice Logic Distribution			
Number of occupied Slices	1,029	7,200	14%

Figure 3.20: Vernier delay line TDC implementation.

Chapter 4

Test environment

4.1 Introduction

In the following, a description of the elements composing the test environment is done. These elements are:

- the TDC tester board, where the FPGA implementation of the time to digital converters is achieved;
- the VME board, hosting the TDC tester board;
- the CPU board Motorola MVME6100 [48], used to read out the TDCs by the VME interface;
- the Rubidium atomic oscillator Symmetricom 8040C [49], used as clock reference;
- the pulse generator Tektronix DTG5334 [50], used to generate the time intervals to be measured by the TDCs;
- the Xilinx MicroBlaze Embedded soft processor [51], implemented in the TDC FPGA and used to monitor the environment physical operating parameters.

The high speed digital design of the TDC tester and VME board implies a field of study half-way between digital design and analog circuit theory. This study is mandatory in order to achieve fast digital hardware working at high frequency.

In the past, the digital systems were made by gates that switched slowly, so the analog modeling of signal propagation was not necessary. At today's speeds even the simple, passive elements of a high speed design, as wires, PCB, connectors and chip package, can make up a significant part of the overall signal delay.

The signal integrity analysis is aimed at the study of the signal lines interference and at the study of the supply voltage and grounding noises of active circuits. It is a challenging building block of the digital design flow and it is essential to the proper operation of every high speed digital board.

4.2 PCB signal integrity analysis

In order to draw a PCB performing picoseconds temporal measurements, an accurate analysis of the analogue features of signal integrity issues and their impact on the design must be carried on. In this high frequency scenario, elements such as connectors, traces and IC (Integrated Circuit) packages may significantly contribute to the delay and the degradation of the signals and the interactions between them. Moreover, waveform distortions and interferences experienced by the switching signals can affect the TDC measurements.

High speed digital design must take into account the circuit passive elements, the interactions between signal and interactions with the surrounding environment. The circuit passive elements affect the signal propagation and may cause ringing and reflections. The interactions between the signals are responsible for crosstalk while the interactions with the surrounding environment may generate electromagnetic interference [52].

Figure 4.1 shows a diagram of an ideal signal and the signal measured with an oscilloscope on a PCB, whose performances deviates significantly from the ideal behavior.

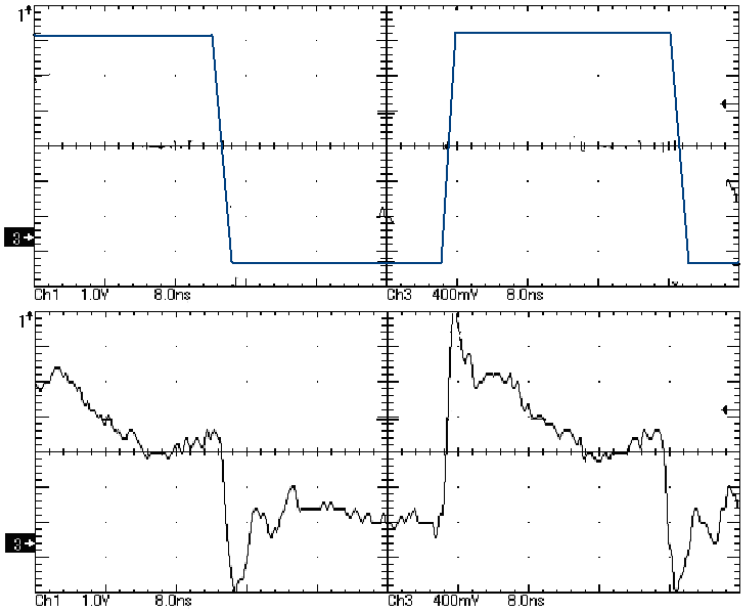


Figure 4.1: Top: ideal signal. Bottom: real signal (1 V/div, 8 ns/div).

The inductance of an IC pin may create a problem that is known as ground bounce or oscillation of the reference ground. This phenomenon causes abnormal levels of the IC output signals whenever the large part of them are simultaneously switching. Figure 4.2 shows the wiring diagram of a typical output stage of a CMOS device with a capacitive load.

The parasitic inductance L1, L2 and L3 generates a voltage drop between the IC ground pin and the PCB reference ground. The voltage drop is proportional to the time derivative of the current flowing through the pin:

$$V_L = L\frac{di}{dt} \qquad (4.1)$$

If the output stage is driving a logic 1, the capacitor representing the load is at the high voltage level. When the output is switched from logic 1 to logic 0, the capacitor is suddenly discharged through the output pin and the IC ground to the PCB ground. This sudden current changing, in combination with the inductance of the IC package pin and of the PCB trace generates IC ground voltage oscillations. The increasing of the ground bounce may introduce transmission errors.

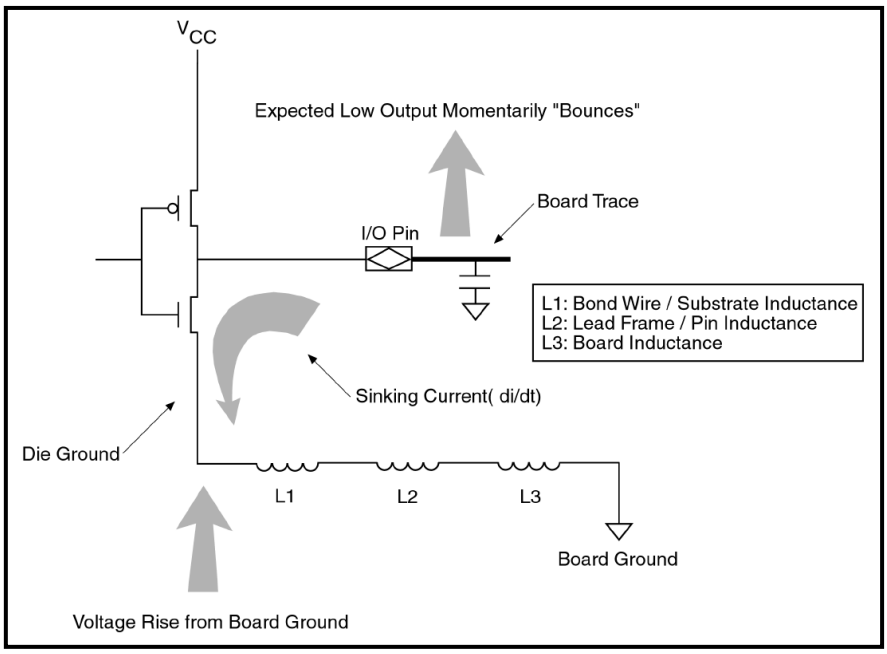


Figure 4.2: Ground bounce model.

In fact, the ground reference of the transmitting device could be different from the ground reference of the receiving one; it implies that a low logic level of the transmitter could be considered an high logic level from the receiver.

The ground bounce may be increased by the following causes:

1. not enough bypass capacitors;
2. a wrong choice of such capacitors which could have high parasitic inductance values;
3. wrong PCB geometry;
4. a large number of simultaneously switching output lines.

Figure 4.3 shows the output signals of a device; a signal is constantly switching, while the other one is set to a low logic level. The ground bounce is clearly visible, in fact the device ground reference is not stable during the switching from high to low of the outputs.

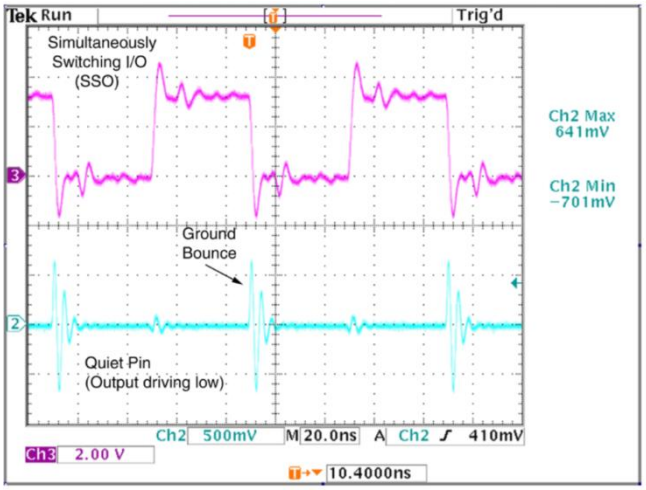


Figure 4.3: Ground bounce (500 mV/div, 20 ns/div).

Moreover, noise is also visible during the output switching from low to high; it is due to the transient current flowing through the output stage when the lower MOSFET (Metal Oxide Semiconductor Field Effect Transistor) stops to draw the current; the value of such current is small and doesn't produce relevant changes of voltage.

New generation devices, as Virtex-5 FPGA, are continuously offering better driving capabilities and are less prone to suffer from ground bounce, but instantaneous power surges still add jitter and change the propagation delay of the signals. Jitter is the deviation of the transition points of a signal from their ideal locations in time [53].

The PCB plays a key role in delivering a stable supply voltage for active circuits and should ensure the signal integrity between devices [54]. The current surge of a digital device changes over time and the changing occurs at different frequency values extending till the first harmonics of the system clock. The power distribution system must be able to meet these fast changing in current consumption with a smallest change of the load voltage.

Figure 4.4 shows the components of the power distribution system; they are the voltage regulator, the decoupling capacitors and active device being powered. In the diagram are also displayed the unavoidable parasitic inductance of the system. They are made by the parasitic inductance of the capacitor and are introduced by PCB vias and traces.

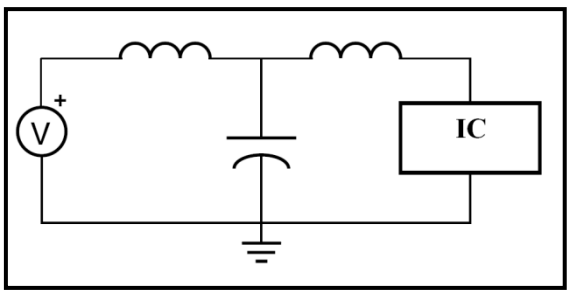


Figure 4.4: Simplified diagram of the power distribution system.

The parasitic inductance slows down changes in current flow; so the capacitor cannot respond instantaneously to transient current or to changes that occur at higher frequency. This effect must be minimized.

Figure 4.5 shows the parasitic model of a real capacitor; it is an RLC circuit (a circuit consisting of a resistor ESR, an inductor ESL and a capacitor C connected in series).

Figure 4.6 shows a real capacitor's impedance characteristic. Overlaid on this plot are curves corresponding to the capacitor's capacitance and parasitic inductance. This two curves combine to form the RLC circuit's total impedance characteristic.

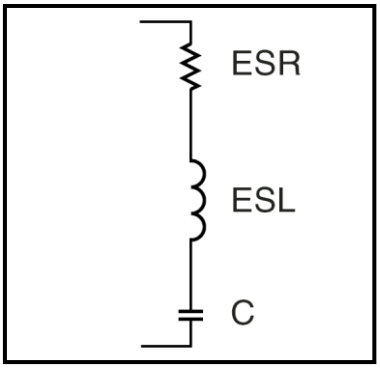


Figure 4.5: Parasitic model of a real capacitor.

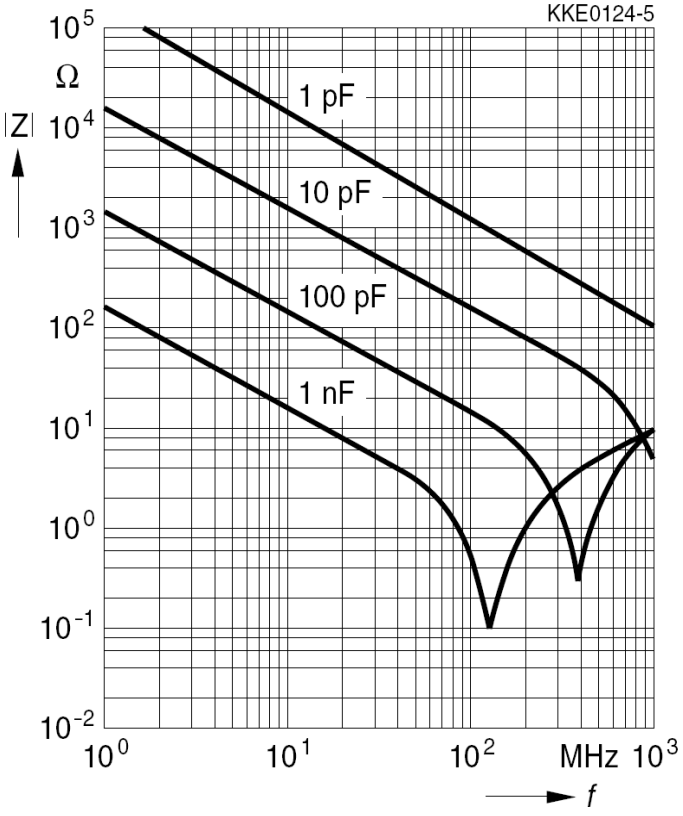


Figure 4.6: Real capacitor's impedance characteristic.

Each capacitor has a limited center band frequency in which it is more decoupling effective. This frequency band corresponds to the resonant frequency of the capacitor and it has to be as high as possible:

$$F = \frac{1}{2\pi\sqrt{LC}} \qquad (4.2)$$

The parasitic inductance of current paths in the PCB have two distinct sources: capacitor mounting (parasitic inductance of traces, vias and capacitor's solder lands on the PCB) and PCB power and ground plane. The vias, traces and capacitor mounting pads contribute inductance between 300 pH to 4 nH depending on specific geometry.

Because the current path's inductance is proportional to the loop area the current traverses, it is important to minimize this loop size. The loop consists of the path through one power plane, up through one via, through the connecting trace to the capacitor, through the capacitor, through the connecting trace to the ground, down through the other via, and into the ground plane, as shown in figure 4.7. The capacitors must be placed very close to the power pin of the chip and the capacitance values must be enough to sustain the supply current for a few nanoseconds. They must have also a low parasitic resistance and inductance values.

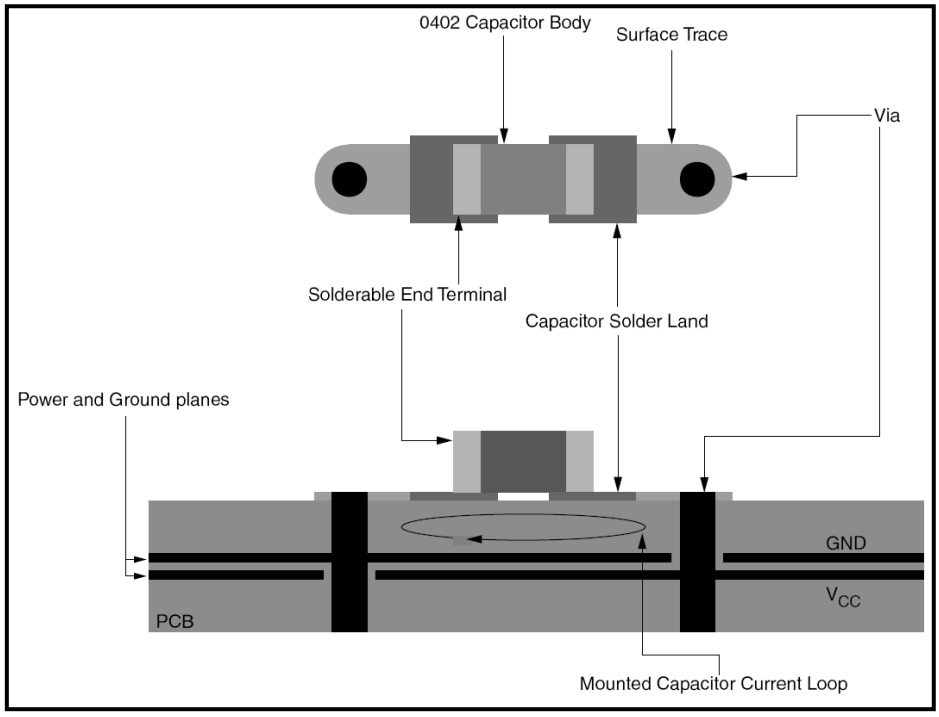


Figure 4.7: Example cutaway view of PCB with capacitor mounting.

The following formula can be used to determine the inductance of the via from its height h, and diameter d (the dimension are in inches and nH):

$$L = 5.08 \times h \times \left[\ln\left(\frac{4 \times h}{d}\right) - 0.75 \right] \qquad (4.3)$$

Some inductance is associated with the PCB power and ground plane. This is described as spreading inductance. Decreased spreading inductance corresponds to closer spacing between the power and ground planes and besides offering a low inductance current path, this design also offer some high frequency decoupling capacitance. Tables 4.1 shows approximate values of spreading inductance for different thickness of FR4 dielectric. The spreading inductance is specified in units of pH per square.

Dielectric Thickness		Inductance	Capacitance / unit area	
(micron)	(mil)	(pH/square)	(pF/in^2)	(pF/cm^2)
102	4	130	225	35
51	2	65	450	70
25	1	32	900	140

Table 4.1: Capacitance and spreading inductance values for different thickness of FR4 dielectric (ε_r= 4.70 max, 4.35 @ 500 MHz, 4.34 @ 1 GHz).

The crosstalk is the interference between signals generated by the coupling between the lines; it can be reduced increasing the distance between them.

The following model shows how the mutual impedance between microstrip lines generates crosstalk on a PCB [55].

Figure 4.8 shows an example of two coupled microstrip lines over a common ground plane, and also shows a generic circuit model for coupled lines. For simplicity, I assume that lines are lossless, then the series resistance and the parallel conductance per unit length will be neglected. The coupling between the lines is modeled by introducing a mutual inductance and capacitance per unit length, L_m and C_m. In the following is assumed that the lines are identical, so they have the same value of capacitance and inductance per length; furthermore it is also assumed that both the lines are terminated at common generator and load impedances, that is Z_{G1}= Z_{G2} and Z_{L1}= Z_{L2}. The generator voltages V_{G1} and V_{G2} are assumed to be different.

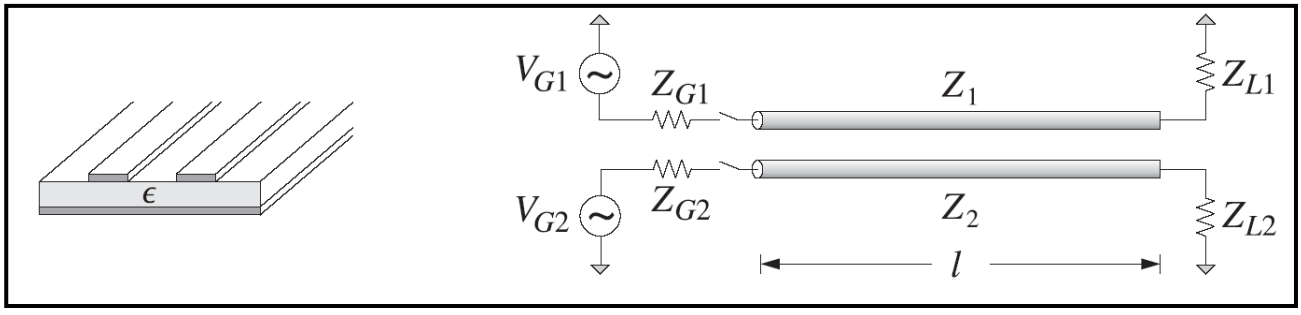


Figure 4.8: Coupled transmission lines.

When only line-1 is energized, that is, $V_{G1} \neq 0$, and $V_{G2} = 0$, the coupling between the lines induces a propagating wave in line-2, referred as crosstalk, which also has some minor influence back on line-1. The near-end and far-end crosstalk are the values of $V_2(z)$ at z=0 and z=l, respectively. The crosstalk expressions simplify drastically if weak coupling is assumed, that is, to first order, line-2 does not act back to disturb line-1:

$$V_2(0,t) = K_b\left[V(t) - V(t-2T)\right] \quad \text{near-end crosstalk} \qquad (4.4)$$

$$V_2(l,t) = K_f \frac{dV(t-T)}{dt} \quad \text{far end crosstalk} \qquad (4.5)$$

where K_b and K_f are known as the backward and forward crosstalk coefficients, T is the propagation time along the uncoupled lines and $V=V_{G1}/2$.

$$K_b = \frac{v_0}{4}\left(\frac{L_m}{Z_0} + C_m Z_0\right), \qquad K_f = -\frac{v_0 T}{2}\left(\frac{L_m}{Z_0} - C_m Z_0\right) \qquad (4.6)$$

where v_0 is the propagation velocity of the signals along the uncoupled lines; it may replace $l=v_0T$. Far-end crosstalk has both polarities, while the near-end crosstalk has the same polarity of the signal generating it. The amplitude of far-end crosstalk is proportional to the slew rate of the signal, its duration is given by the signal rising time. The amplitude of far-end crosstalk is a fraction of the output signal amplitude. Crosstalk can be reduced by increasing the spacing between the lines and decreasing the distance from ground planes, because this kind of layout minimize the mutual inductance and capacitance of the coupled lines.

Figure 4.9 shows the signals for a pair of coupled lines matched at both ends. The uncoupled line impedance was $Z_0=50\ \Omega$.

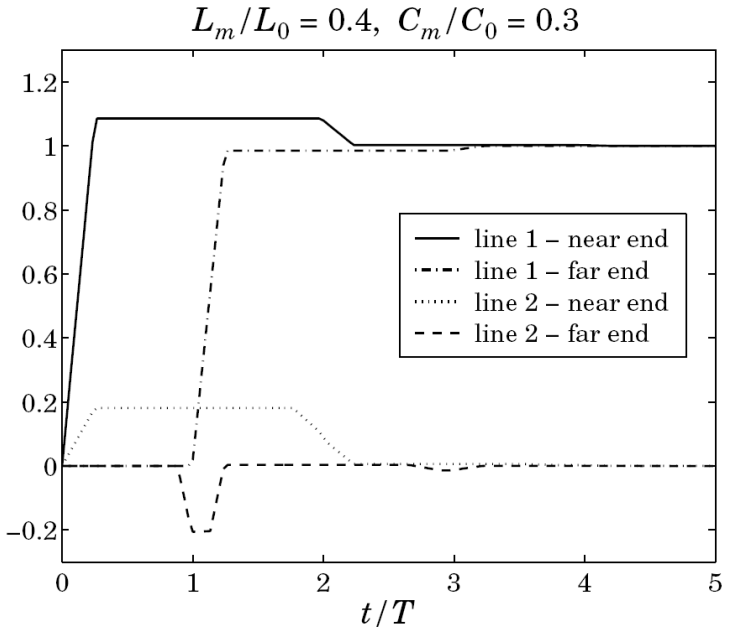


Figure 4.9: Near-end and far-end crosstalk signals on lines 1 and 2.

4.3 TDC tester board

In order to test the TDC architectures on the field, I have designed and built the TDC tester board shown in figure 4.10. This board is designed around a Xilinx Virtex-5 FPGA. The two different TDC architectures can be used changing the firmware installed on the FPGA configuration memory. The in-system programming and reconfiguration features allows the designer to generate many trial and error iterations of the design before finding the optimal design.

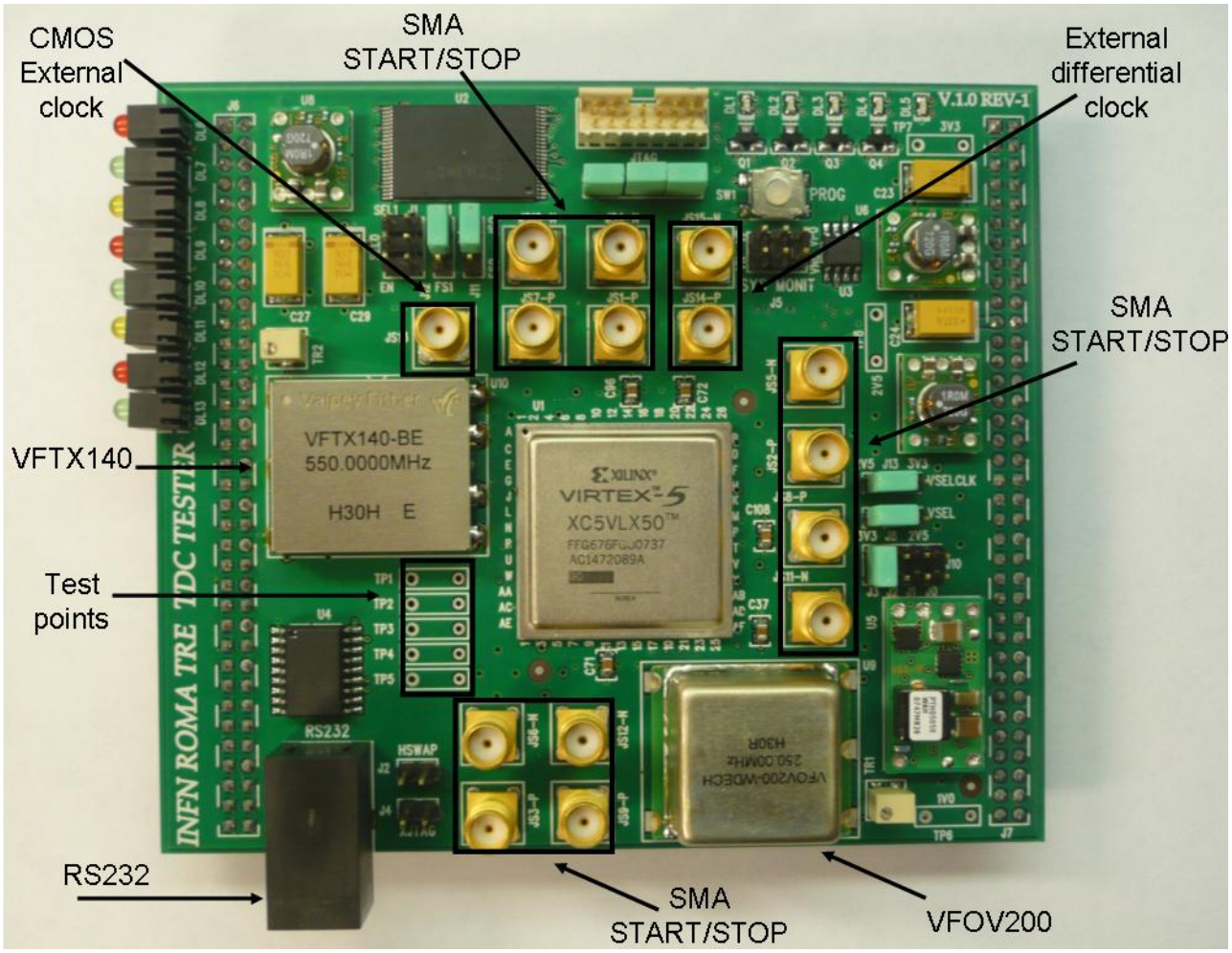


Figure 4.10: TDC tester board.

The tester board has a ten-layer stackup with multiple ground planes and adopts a stripline layout. On this board I have installed two high stability oscillators [56]. The first oscillator (VFTX140) generates an output frequency of 550 MHz. Its temperature stability is better than 0.28 ppm over a temperature range from 0°C to + 70°C. The output is configured as a differential LVPECL signal. Long term time accuracy depends on the oscillator stability. To address this problem the VFOV200 oscillator has been selected. This oscillator provides an HCMOS (High speed Complementary

Metal Oxide Semiconductor) output frequency of 250 MHz and it has a temperature stability up to 5 ppb over a temperature range from -40°C to +85°C. Furthermore SMA (Sub Miniature version A) connectors are used to deliver external CMOS and differential clocks to the TDC in order to compare the high stability oscillator performance on long range measurements with an atomic oscillator reference or simply in order to use commercial oscillators.

Test points for high bandwidth active probes are used to perform the Virtex-5 clock signal characterization. SMA connectors are used to send the start and stop signals to the device. They may adopt differential or single-ended signaling schemes. These signals path skew is within 20ps and it is removed by the calibration procedure.

An RS232 connector has been installed in order to read out the TDC also by means of the MicroBlaze embedded processor which is a soft processor implemented in the Virtex-5 FPGA.

The Virtex-5 FPGA contains a system monitor [57] located in the center of the die. This monitor is built around a 10 bit ADC (Analog to Digital Converter). I have used this function to monitor the temperature and the power supply voltages (V_{CCINT}, V_{CCAUX}). These parameters were acquired, by VME, together with the time measurements; they can also be acquired by means of the MicroBlaze processor in order to perform a real time calibration of the fine TDC.

Great attention has been paid to the signal integrity issues of the board due to the high frequency design, in order to limit ground bounce, crosstalk and transmission line problems.

4.4 VME board

The tester daughter board is hosted in a VME (Versa Module Europe) module, shown in figure 4.11, which allows to test and read out the TDC via a VME off-the-shelf CPU board, the Motorola MVME6100. The VME board can handle A32/D16 VME cycles and is configured as slave; it is designed around a Xilinx Spartan IIE FPGA clocked by an on-board 40 MHz oscillator. The board may also implement the fastest A64/D64 2eSST (Double-Edge Source Synchronous Block Transfer) cycles (320 MByte/s), for future data acquisition upgrades, according to the firmware installed on the FPGA configuration memory.

The 2eSST is the latest performance update of the VME64 protocol, approved as an ANSI standard in 2003 [58]. This extension has taken the VME data transfer rate from the original 40 MByte/s to 320 MByte/s.

The architectural change at the base of such an impressive step forward is twofold. Different from all the previous cycles, data transfers are driven synchronously by the producer, without handshaking, and data is latched on both the rising and falling edges of the strobe signal.

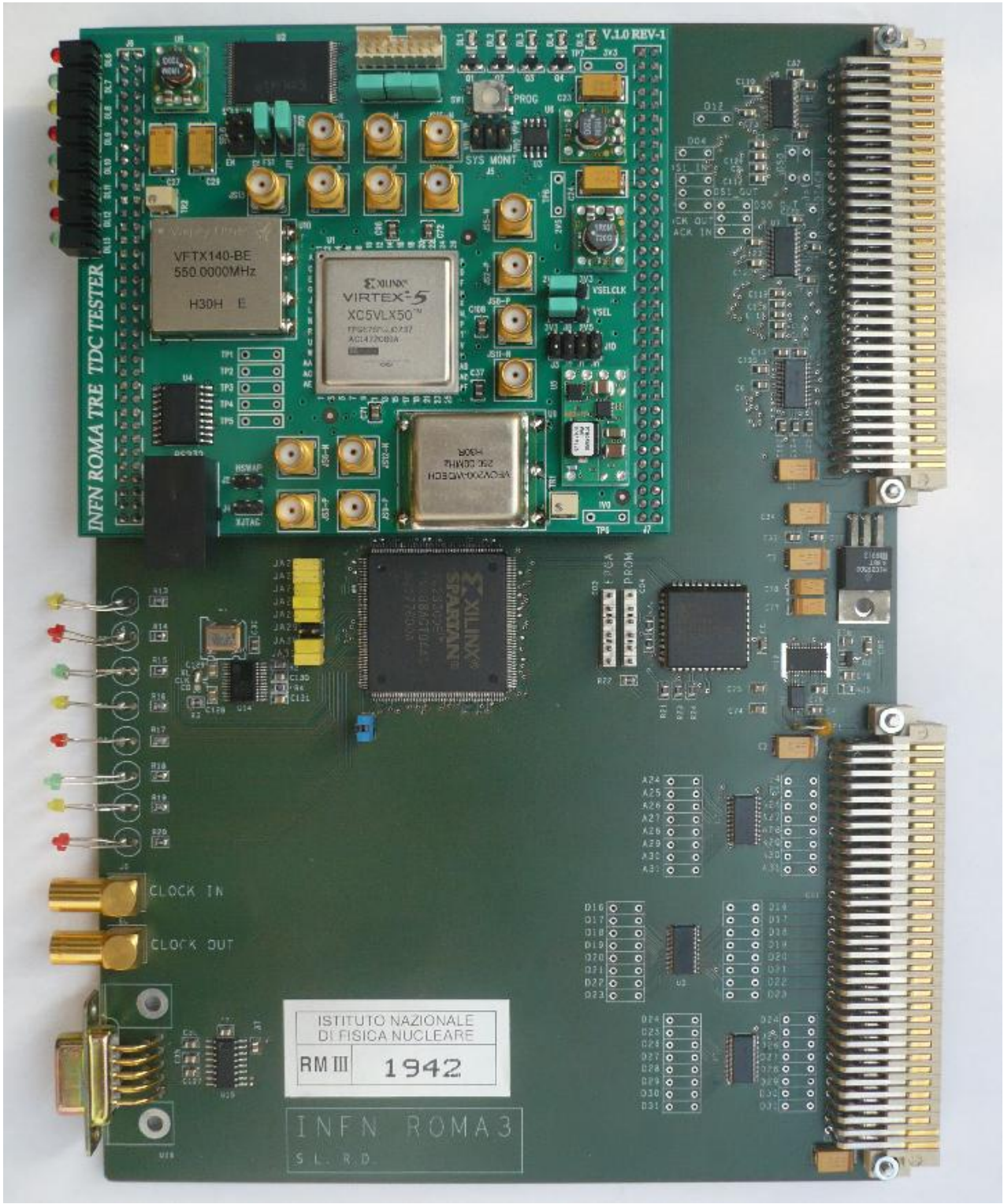


Figure 4.11: VME board.

In this technique, a careful approach to signal integrity has shown to be critical in order to avoid timing violations. The double-edge technique shrinks the signals settling time, halving the transaction cycle with respect to the classic edge-triggered logic. Strobe's duty cycle, crosstalk,

impedance matching and proper line termination, clean power supply are just a few design parameters playing a key role in the design of a high speed double edge board.
Beside the data integrity, the strobe timing plays a crucial role in the 2eSST protocol. The strobe edge can be moved away from its original position by noise sources, like ground bounce, power supply fluctuations, pattern-dependent effects, crosstalk and other interferences.
This timing jitter can be responsible for subtle malfunctions, marginal behaviors and intermittent timing violations quite hard to track down.

4.5 MVME 6100

The Motorola MVME6100 is a CPU board equipped with the latest VME controller available on the market. The Tundra TSI-148 [59] interface chip implements all the cycles defined by the VME protocol, including the asynchronous and synchronous double edge block transfers and legacy cycles as well.
The CPU board is designed around the MPC7457 PowerPC processor running at 1.267 GHz. The on-board peripherals are connected through a Host Bridge supporting two 133 MHz/64 bit PCI-X and the 133 MHz PowerPC processor and memory busses. This architecture provides balanced performance to and from the processor, I/O units, local busses and memory. The board can handle the 320 MByte/s (40 MHz/64 bit) VME data traffic sustained by the 2eSST without saturating the internal aggregate bandwidth.
A software development kit is available from SYSGO [60], which allows customizing and porting a LINUX distribution specifically tailored for the user's application. In my setup, the board has been configured as a diskless node, booting via the network from a PC running LINUX. The board downloads the Kernel and a bundle of user's application, including a resident C/C++ compiler.
The TSI-148's driver provided by SYSGO has been modified in order to map the VME bus address space into user's memory. This approach disentangles the developer from the physical device, simplifies the software development and improves portability to different platforms.

4.6 Rubidium frequency standard

The TDC measurements are also used to compare the on board high stability oscillators performances with an atomic oscillator reference, the Symmetricom 8040C. It is designed around a rubidium oscillator and provides a stable and accurate frequency reference. It has six outputs, each of which provides a 10 MHz square wave or 1PPS output and a RS232 interface for command and control.

A 1PPS input allows the 8040C to be disciplined by a GPS receiver for improved frequency accuracy and long-term stability. The 8040C auto adaptive algorithm allows plug and play connectivity for easy GPS disciplining.

Table 4.2 and table 4.3 show the performance parameters of the Symmetricom 8040C for the low phase noise version I used:

Avg. time (s)	Allan deviation
1	<1.5E-11
10	<8E-12
100	<2.5E-12

Table 4.2: Stability.

Avg. time (s)	Allan deviation
1 month	<5E-11
1 year	<5E-10

Table 4.3: Aging.

4.7 Test setup

To perform the tests I have used an architecture based on the Motorola MVME6100. The VME board hosting the TDC Tester daughter card can handle A32/D16 VME cycles and is configured as slave. In the first setup, I have used a Tektronix DTG5334 as a pulse generator. It is a data timing generator and it can deliver time intervals as long as 20 μs in 1 ps steps. Since we have operated the DTG in free running mode, an accept signal was delivered by the MVME6100 to the VME slave board in order to start and stop measurements. This test set up is shown in figure 4.12.

In order to test long term accuracy I have used a different architecture; it is also based on the Motorola MVME6100 to read out the TDC. Figure 4.13 shows the simplified block diagram of the second VME setup.

In the second setup the CPU board is also used to address an I/O register employed to generate several delays, ranging from nanosecond until seconds, between the start and the stop signals.

The time interval between start and stop has been determined by the CPU clock; in fact it is the time elapsing between the write cycles of the CPU to the I/O register. This time can be changed by software and then it is measured by two different TDC tester boards.

According to the firmware installed in the FPGAs configuration memory, one is synchronized by a 10 MHz Rubidium atomic oscillator, while the other is synchronized by the high stability 550 MHz LVPECL oscillator. The external Rubidium clock frequency is multiplied in the FPGA by using the Virtex-5 Digital Clock Managers (DCMs) in order to have a 480 MHz clock frequency. I compared the two TDC tester boards performance side by side.

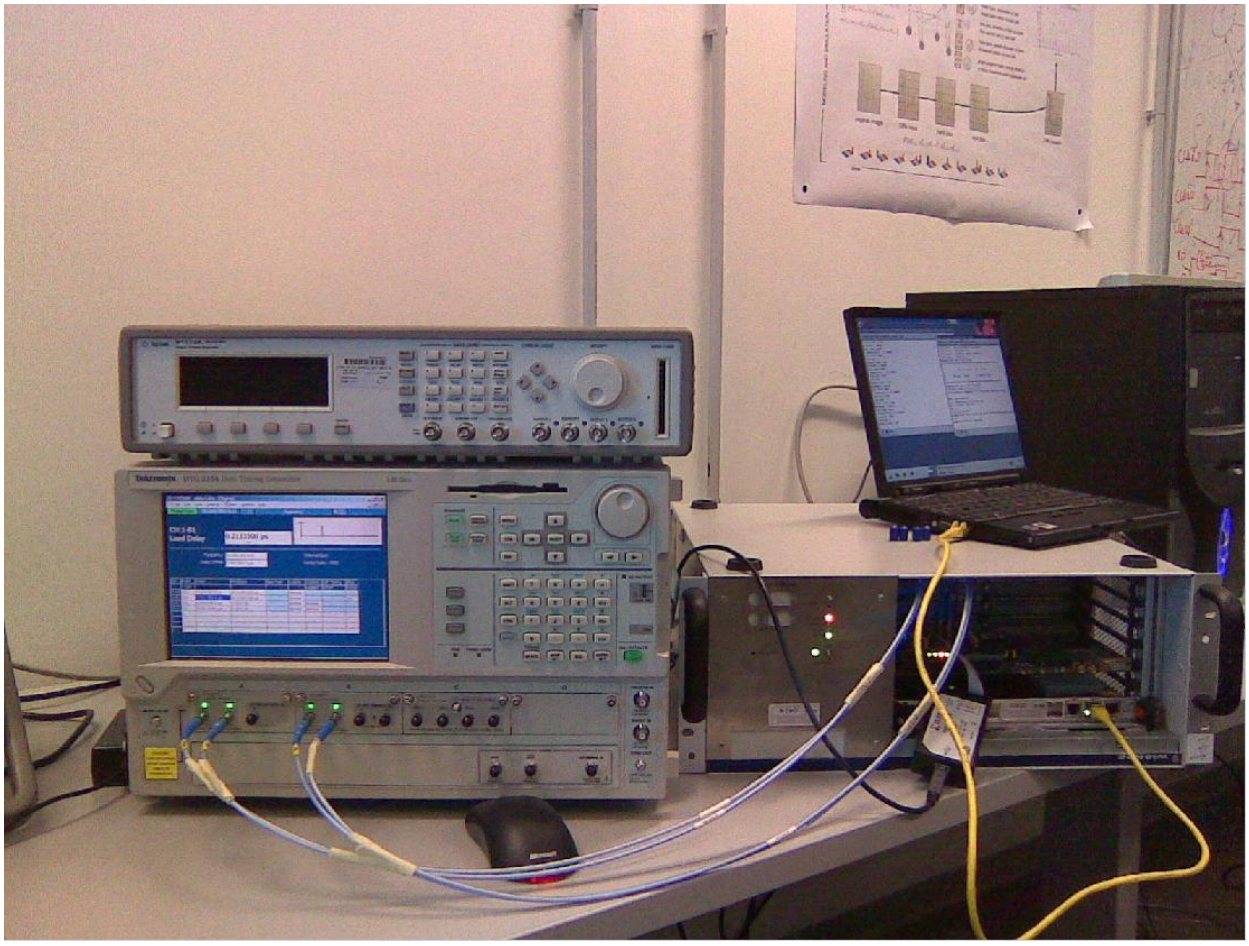


Figure 4.12: First VME setup.

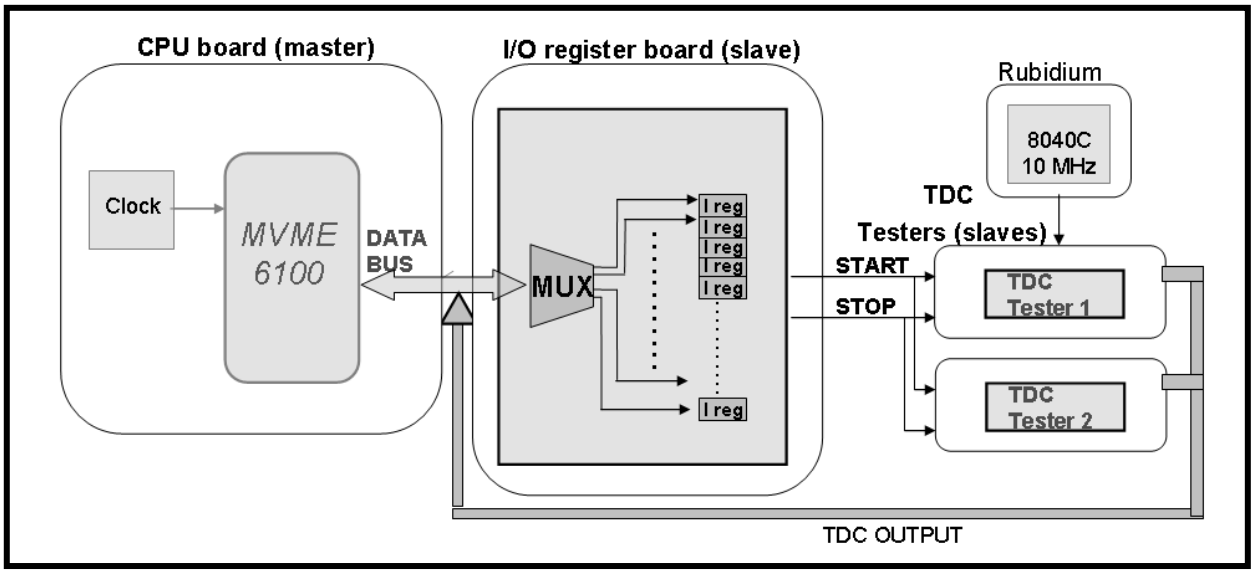


Figure 4.13: Simplified block diagram of the second VME setup.

4.8 FPGA physical operating parameters measurements

The physical operating parameters measurements are made by means of the Virtex-5 system monitor. It is built around a 10 bit, 200 kSPS (kilosamples per second) ADC and it is located in the center of the device. I have used it to measure the on chip power supply voltages VCCINT and VCCAUX and the die temperature. A state machine implemented in the Virtex-5 FPGA allows to set the system monitor control registers in order to perform monitoring of the physical parameters. 256 individual readings are averaged to ensure robust noise-free measurements. The result of the VCCINT, VCCAUX and temperature averaged values are then placed in three registers every 8 ms. The LSB value of the temperature reading is about 0.49°C, the LSB value of the voltages reading is 2.93 mV.

The VCCINT, VCCAUX and temperature registers can be read by VME or by the MicroBlaze soft processor implemented in the FPGA. The MicroBlaze firmware, I have implemented, allows the user to manage the processor via an RS232 link.

The MicroBlaze embedded processor soft core is a Reduced Instruction Set Computer (RISC) optimized for implementation in Xilinx FPGAs. Figure 4.14 shows a functional block diagram of the MicroBlaze core.

The feature set of the processor includes 32 general purpose 32 bit width registers, 32 bit instruction word with three operands and two addressing modes, 32 bit address bus and single issue pipeline.

In addition to these fixed features, the MicroBlaze processor is parameterized to allow selective enabling of additional functionality.

The processor can reach operating frequency of about 235 MHz on Virtex-5 FPGAs; the maximum performance and maximum clock frequency varies from one design to another, according to the configuration options used.

The processor is implemented with a Harvard memory architecture; instruction and data accesses are done in separate address spaces. Each address space has a 32 bit range (that is, handles up to 4 GB of instructions and data memory respectively). Both instruction and data interfaces of MicroBlaze are 32 bits wide and use big endian, bit reversed format. The processor does not separate data accesses to I/O and memory (it uses memory mapped I/O). It has up to three interfaces for memory accesses:

- Local Memory Bus (LMB)
- Processor Local Bus (PLB) or On chip Peripheral Bus (OPB)
- Xilinx CacheLink (XCL).

The LMB memory address range must not overlap with PLB, OPB or XCL ranges.

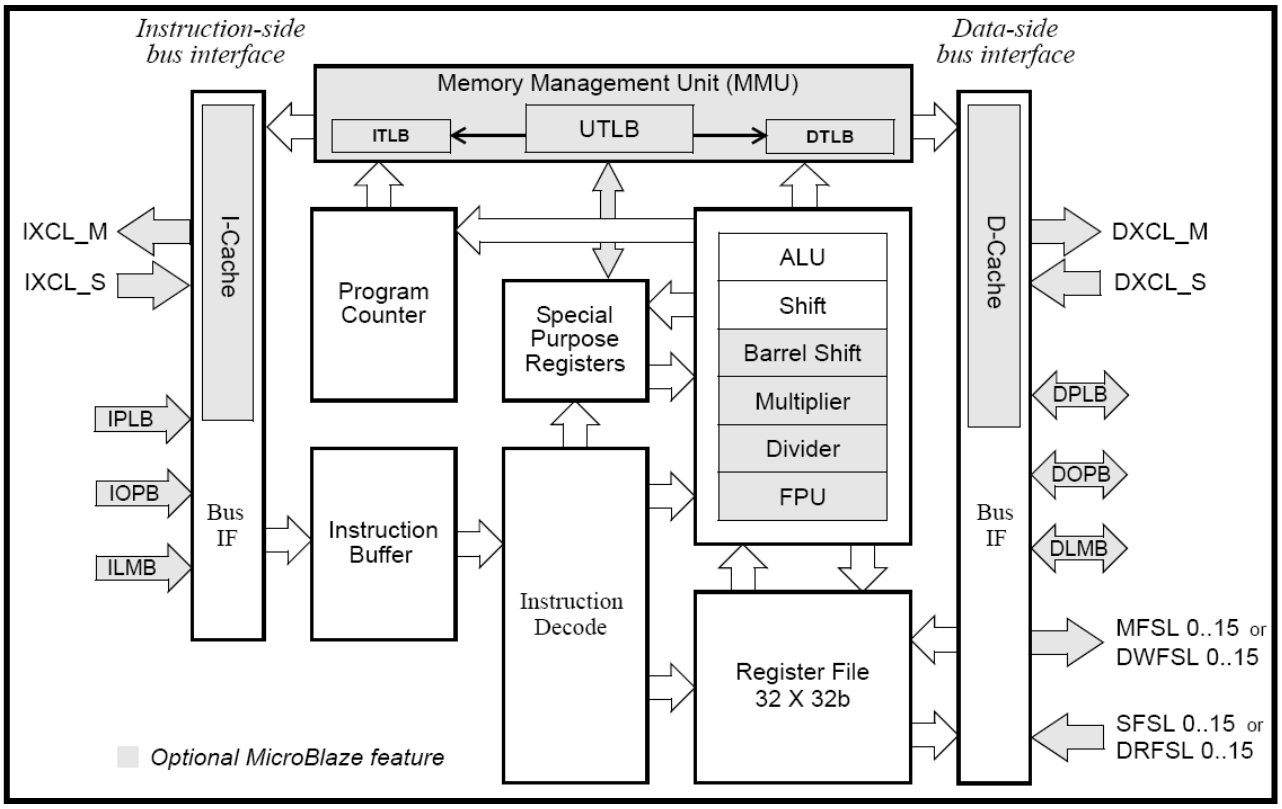


Figure 4.14: MicroBlaze Core Block Diagram.

The LMB has a 32 bit width and is used for low latency access to on chip block RAM. The LMB provides single cycle access to on chip, dual port block RAM and it is split into Instruction side LMB (ILMB) and Data side LMB (DLMB). It is a synchronous protocol and provides maximum guaranteed performance of 210 MHz in Virtex-5 FPGAs for the local memory subsystem.

If needed, off chip memory is accessed via the PLB; it is a 32 bit version of the PLB v46 interface [61]. The PLB v46 supports dynamic bus sizing as well as programmable burst size, it is split into Instruction side PLB (IPLB) and Data side PLB (DPLB).

MicroBlaze can be configured also with the OPB interface; it is a 32 bit version of the OPB v2.0 bus interface [62]. OPB is split into Instruction side OPB (IOPB) and Data side PLB (DOPB).

Caches are implemented with FPGA block RAM. The MicroBlaze processor includes a tightly coupled, off chip Flash/SRAM memory controller interface to provide high speed, low latency access, called CacheLink. The CacheLink interface implements the cache function to external memory without tying up the PLB v46 bus or the OPB v2.0, it is split in Xilinx Instruction CacheLink Interface (IXCL) and Xilinx Data CacheLink Interface (DXCL).

The processor contains sixteen input and output Fast Simplex Link (FSL) interfaces. The FSL interfaces can be up to 32 bits wide; they are unidirectional, non-arbitrated, dedicated communication channels. The FSL is basically a FIFO (First In First Out). In fact, the interface on

the fabric side is that of a FIFO. The master side signals (MFSL) are for the write from fabric direction while the slave side signals (SFSL) are for the write to fabric direction.

Chapter 5

Test results

5.1 Introduction

The TDC architectures approach exploits the classic Nutt method based on multi-stage interpolation. The first stage is built around a coarse free-running counter used to measure long time intervals. The coarse conversion dynamic range is limited by the counter output width. The bin size of the coarse output is limited by the clock period. The second stage is built around a state machine synchronized by the DCM output signals, used to perform a first level phase interpolation thus giving a resolution of a quarter of the clock period. The performances of the first and second stage on the long range time measurements are reported in the paragraphs from 5.2 to 5.4.

The third stage performs the fine time measurement thus improving the coarse counter resolution. Since I also exploit the four phases information delivered by the DCM, the fine time measurement must only interpolate in between the four different phases i.e. over a quarter of the clock cycle. I designed two different fine time converters in order to compare their performances side by side. The first one consists of tapped delay lines and the second one uses Vernier delay lines. The performances of the third stage on the short time measurements are reported in the paragraph 5.5.

In order to test the long range TDC behavior, I used three different oscillators with different long term stabilities; I compared their performances side by side:

1) A 40 MHz commercial quartz, hosted in the VME board and delivered to the TDC tester board. It is multiplied into the FPGA by means of the Virtex-5 DCM in order to generate a 480 MHz frequency;
2) A 550 MHz high stability oscillator, hosted in the TDC tester board.
3) A 10 MHz Rubidium atomic oscillator. It is multiplied into the FPGA by means of the Virtex-5 DCMs in order to generate a 480 MHz frequency.

The Rubidium is considered the most stable of the three oscillators, because of its long term stability and the synchronization with the Global Positioning System.

Hereafter, the TDC synchronized by the 40 MHz commercial quartz is named quartz TDC, the TDC synchronized by the 550 MHz high stability oscillator is named high stability TDC and the TDC synchronized by the Rubidium oscillator is named Rubidium TDC.

The short range fine time measurements are made only with the high stability TDC.

The measurements were made by sampling the FPGA physical operating parameters, such as the on chip power supply voltages VCCINT and VCCAUX and the die temperature, by means of the Virtex-5 system monitor.

In order to ensure robust noise-free measurements, 256 individual readings of the VCCINT, VCCAUX and temperature are averaged. The averaged values are then placed in three registers every 8 ms and are read out, by VME, together with the time measurements. The LSB value of the temperature reading is about 0.49°C, the LSB value of the voltages reading is 2.93 mV. The measured VCCINT and VCCAUX are about 0.993 V and 2.493 V respectively; these values vary within the range of few mV and do not have an effect on the measurements session.

5.2 Preliminary study

The preliminary study is aimed to compare the performances of the quartz TDC and the Rubidium TDC for short range measurements. Since the signals synchronizing the two TDCs have the same nominal 480 MHz frequency, one “coarse count” represents equal amount of time (about 521 ps); so I used the number of counts for comparison.

Figure 5.1 shows the linear relation between the quartz and Rubidium counts. About 200 events are generated for each point and for each event, a time interval to be measured by the quartz and Rubidium TDCs is produced. Only very short time intervals are produced ranging from about 30 ns till 90 ns. The number of counts measured by each TDC in each event is recorded and in figure 5.1 a linear fit, to guide the eye, is superimposed on experimental data.

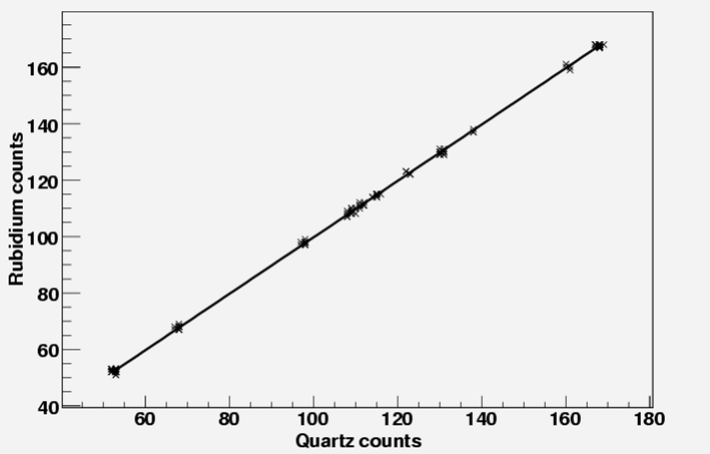


Figure 5.1: Linear relation between the counts measured by the quartz and the Rubidium TDCs.

The quartz TDC maintains reasonably good stability and precision for measurements of time interval within 90 ns.

5.3 Long term stability of the Quartz TDC

I examined the performance of the quartz TDC for measurements of longer time intervals. About 1500 events are generated; throughout the events, the time interval to be measured increases from zero all the way up to 8850 milliseconds in 5,9 milliseconds steps. I did two kind of measurement sessions; the first session is made with the GPS not disciplining the Rubidium oscillator, while the second session is made with the GPS disciplining the Rubidium oscillator.

The measurements of the first session are shown in the figure from 5.2 to 5.4, while the measurements of the second session are shown in the figure from 5.5 to 5.7.

Figure 5.2 shows the difference between the quartz and Rubidium TDCs measurements versus the Rubidium time when the GPS is off.

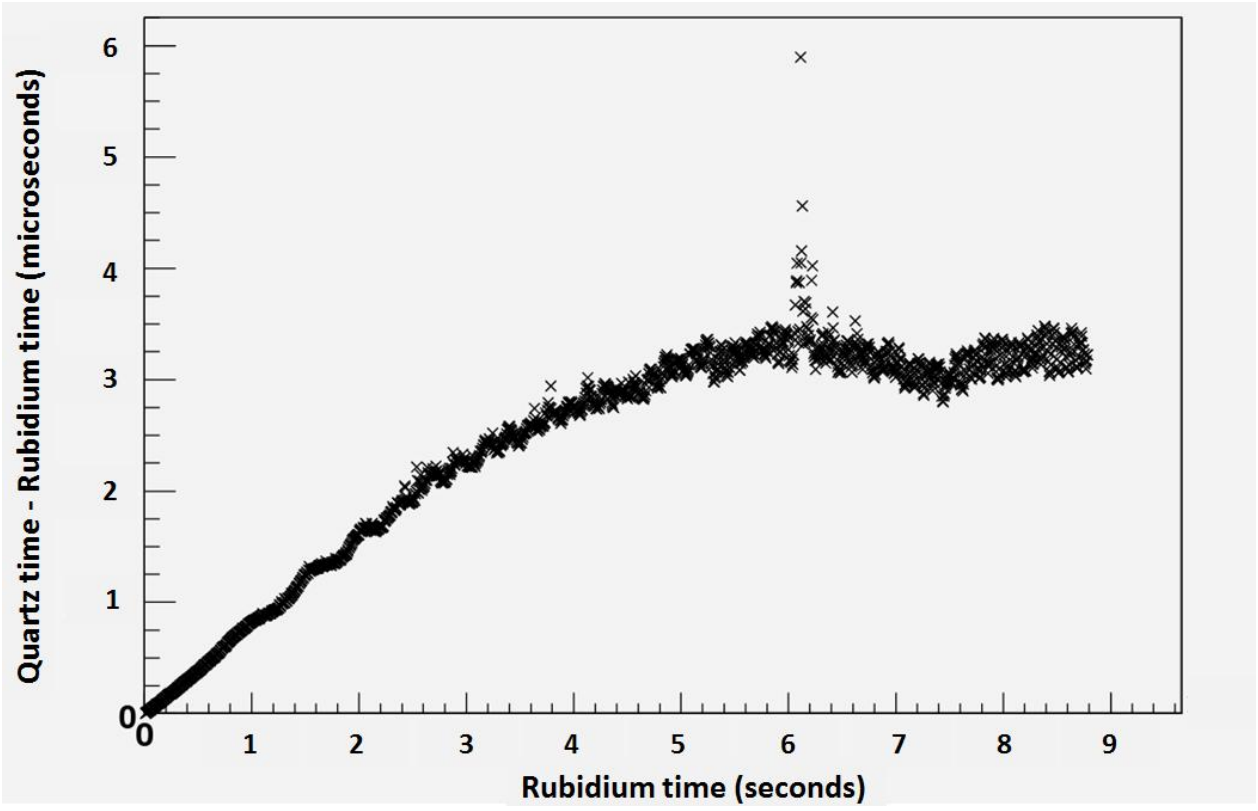


Figure 5.2: Difference between quartz and Rubidium TDCs versus Rubidium time (GPS off).

Figure 5.3 (left) shows the variation of the quartz TDC temperature with event number. Figure 5.3 (right) shows the variation of the Rubidium TDC temperature with event number.

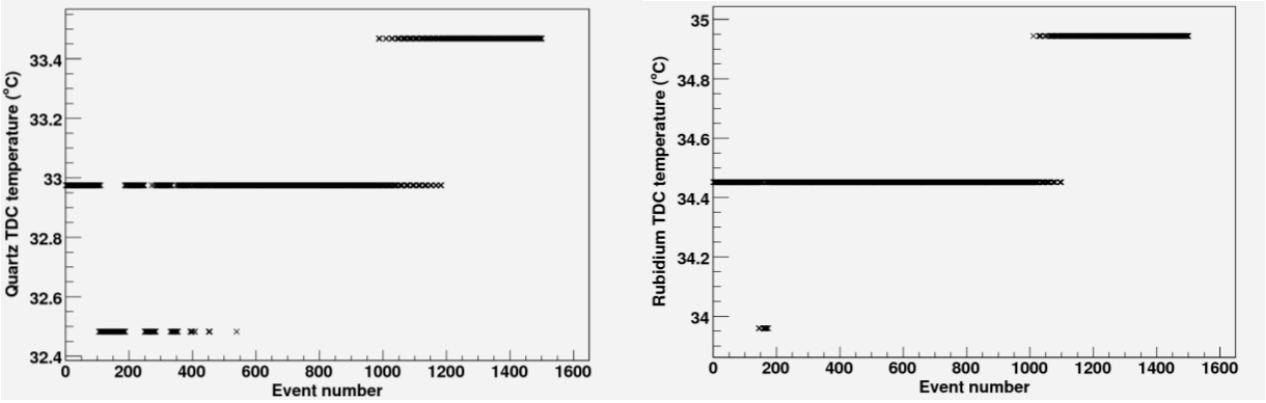


Figure 5.3: Variation of the TDCs temperature versus event number (GPS off). Left: Quartz TDC. Right: Rubidium TDC.

Figure 5.4 shows the difference in temperatures of quartz and Rubidium TDCs as function of the event number.

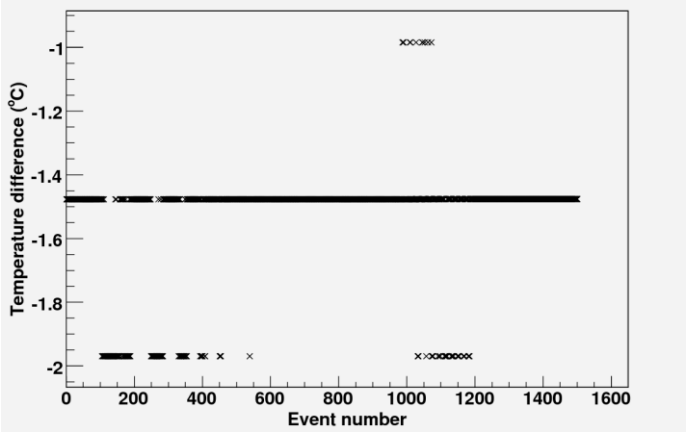


Figure 5.4: Difference in temperatures of quartz and Rubidium TDCs versus event number (GPS off).

As shown in the graphs, the temperatures of the two TDC chips vary within the range of ±1°C, and does not have an effect on the discrepancy between the quartz measurements and the Rubidium measurements. Nonetheless, the oscillatory fluctuations in the graph of the difference between quartz time and Rubidium time is very pronounced for event number higher than 6 seconds (about 1000 events).

Figure 5.5 shows the difference between the quartz and Rubidium TDCs measurements versus the Rubidium time when the GPS is on.

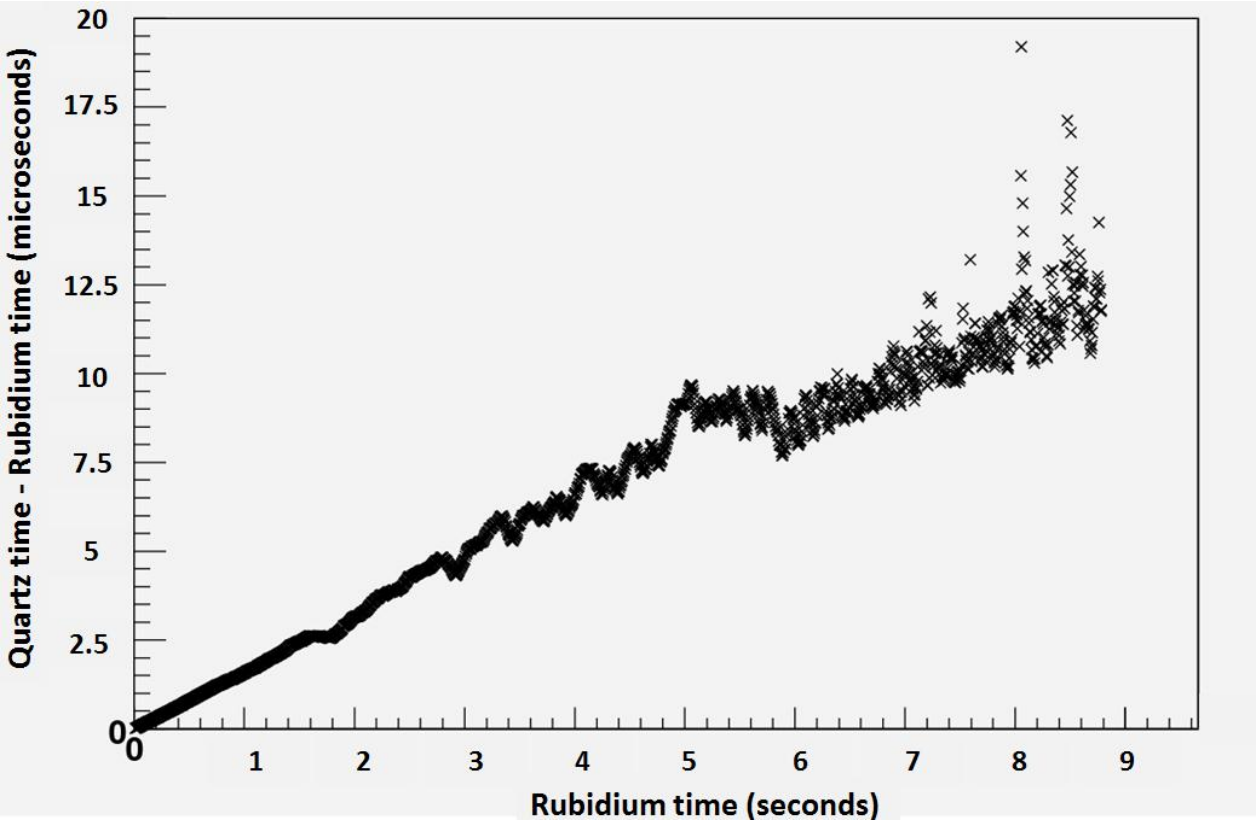


Figure 5.5: Difference between quartz and Rubidium TDCs counts versus time interval (GPS on).

Figure 5.6 (left) shows the variation of the quartz TDC temperature with event number. Figure 5.6 (right) shows the variation of the Rubidium TDC temperature with event number.

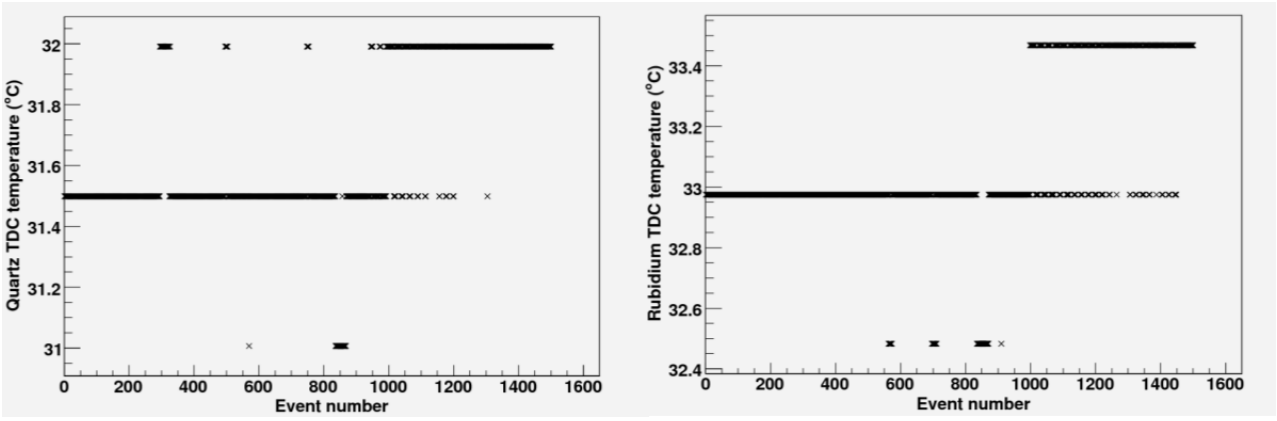


Figure 5.6: Variation of the TDCs temperature versus event number (GPS on). Left: Quartz TDC. Right: Rubidium TDC.

Figure 5.7 shows the difference in temperatures of quartz and Rubidium TDCs as function of the event number.

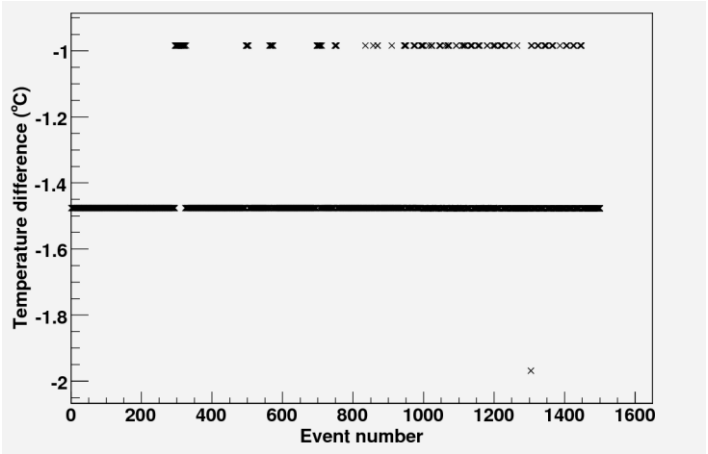


Figure 5.7: Difference in temperatures of quartz and Rubidium TDCs versus event number (GPS on).

Figure 5.8 shows the difference between quartz time and Rubidium time when GPS is on and when the GPS is off. The periodic synchronization of the GPS connected to the Rubidium TDC is a cause of the oscillatory fluctuation; in fact such fluctuation is less pronounced for the curve corresponding to the GPS off.

The tests show that the commercial quartz oscillator can still be used for measurements of short time intervals and measurements that do not require very high precision.

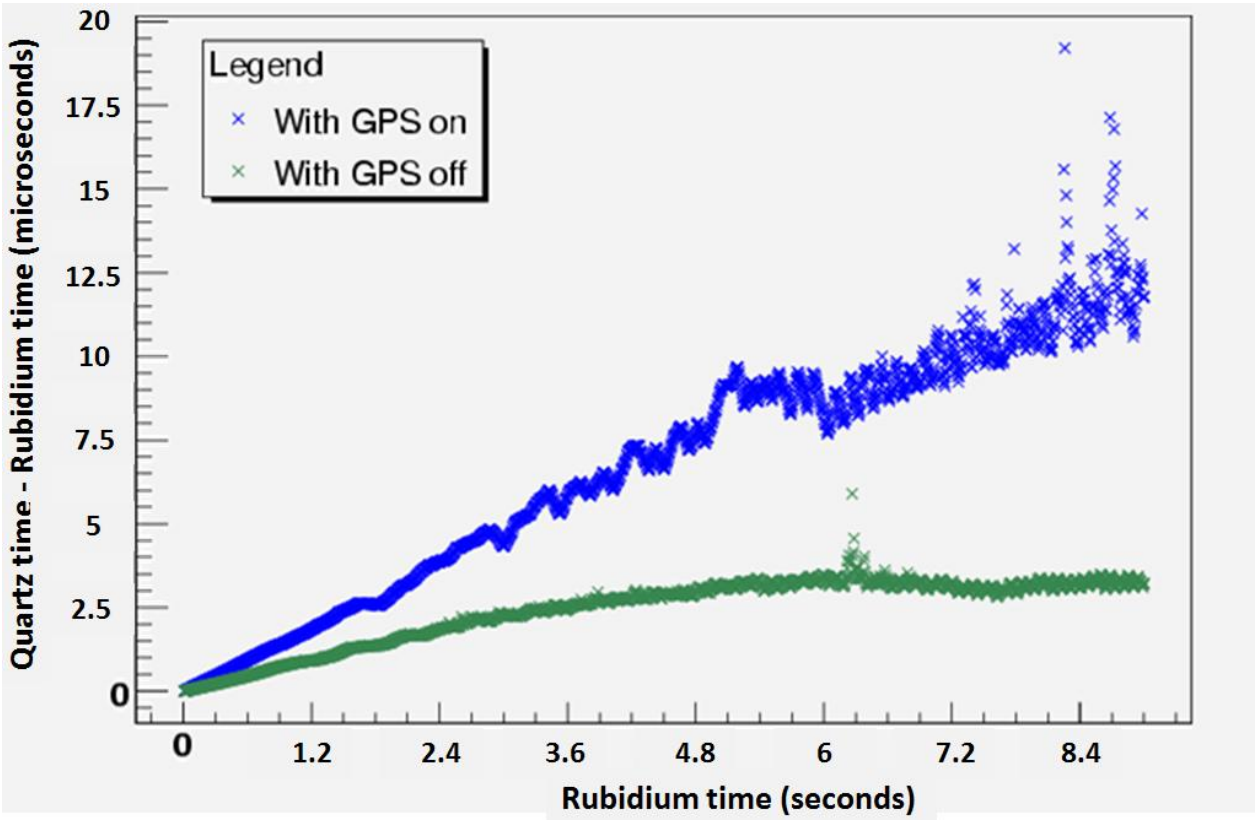


Figure 5.8: Difference between quartz count and Rubidium count when GPS is on and when the GPS is off.

5.4 Long term stability of the high stability TDC

I calibrated the high stability TDC with respect the Rubidium TDC in order to obtain a more precise time measurement. Owing to the difference in the frequencies of the two oscillators, the number of counts is converted into the total amount of time that it represents. In fact for the 550 MHz high stability TDC a count is about 454 ps, while for the Rubidium oscillator a count is 521 ps. Figure 5.9 shows the difference in times measured by the high stability and the Rubidium TDCs. The measurements are made with the GPS not disciplining the Rubidium oscillator.

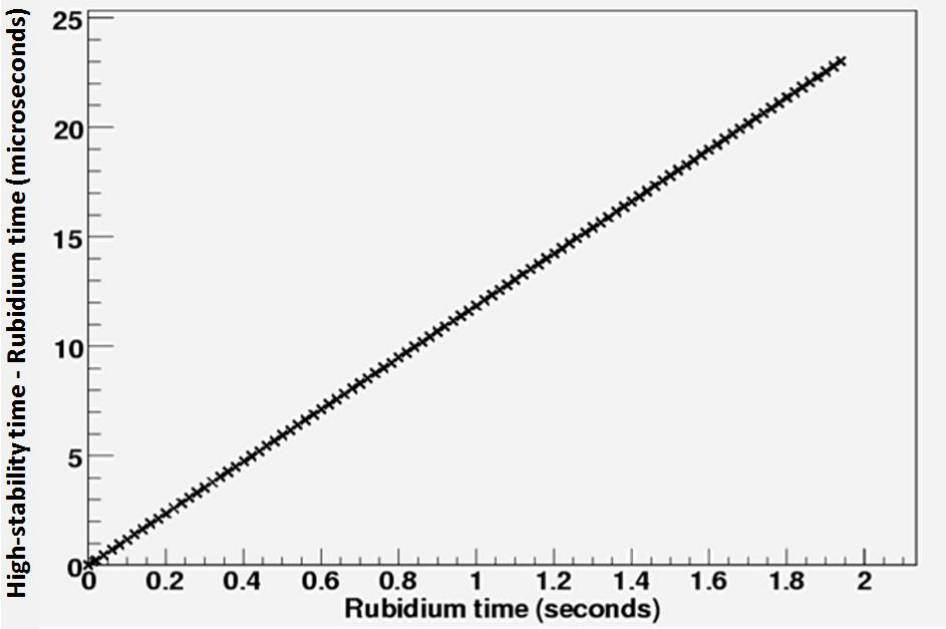


Figure 5.9: Difference in times measured by the TDC synchronized by the high stability oscillator and by the Rubidium oscillator.

In order to test long term time accuracy the time interval to be measured increases from zero all the way up to 2 seconds in 5,9 milliseconds steps.

The high stability TDC maintains reasonably good stability and precision for the entire range of measurements.

5.5 Fine TDC tests

The short range fine time measurements are made only with the high stability TDC synchronized by the 550 MHz high stability oscillator. The tests are aimed to compare the performance of the tapped delay lines used in flash TDC architecture and the Vernier delay lines for short range measurements. The delay lines are used to interpolate the time interval inside a quarter of the clock period of about 454 ps.

5.5.1 The second stage output linearity

I executed tests of the phase occupancy of the rising edge of the start and stop signal within the system clock period for both the architectures. Figure 5.10 shows a plot of the hit counts distribution for the carry chain delay line architecture. 160000 measurements were acquired at a fixed time interval (100 ns). The operating temperature was of about 30 °C. Figure 5.11 shows the same plot for the Vernier delay line architecture. The plots of figure 5.10 and 5.11 are similar because the architecture of the first and second stages of the two TDCs are the same. Start and stop edge integer distribution's interval is numbered from 0 to 3.

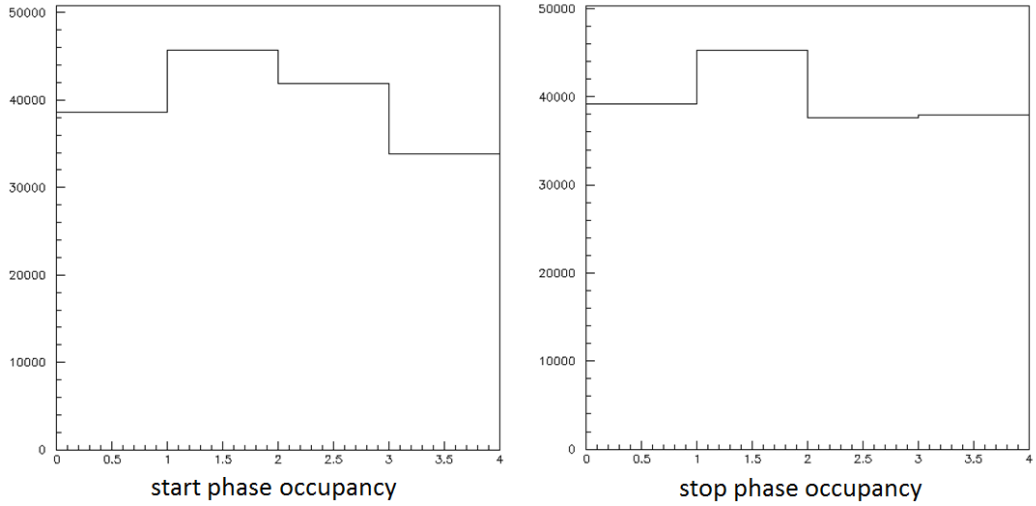


Figure 5.10: Hit counts as function of the phase value for the TDC flash architecture. Left: Start phase occupancy. Right: Stop phase occupancy.

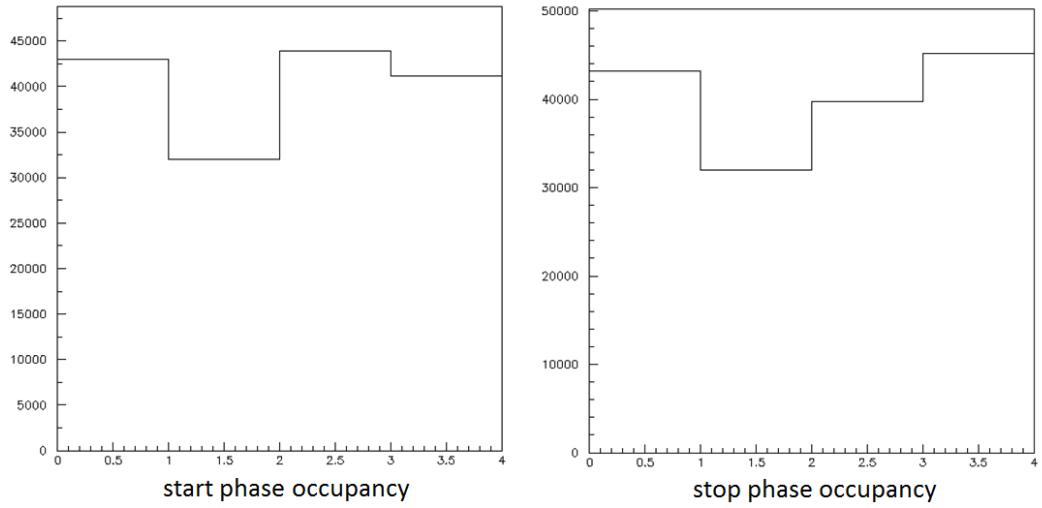


Figure 5.11: Hit counts as function of the phase value for the TDC Vernier architecture. Left: Start phase occupancy. Right: Stop phase occupancy.

The distribution in figure 5.10 and figure 5.11 should be ideally flat, because the rising edge of the start and stop signals have the same probability of happening in every quarter of the clock period. The propagating delays of the start or the stop signals, as shown in figure 3.6, through the synchronizing stages can be different, due to the routing in the FPGA device. The resulting skew of the start or stop signal can bias the measurements and introduces some non-linearity in the phase occupancy of the rising edge of the start or stop signal within the clock period. This non linearity can be expressed by the differential (DNL) and integral (INL) non linearity of the start and stop measurements.

Figure 5.12 and 5.13 show the DNL for the phase occupancy distribution of the start and stop signals for the flash and Vernier delay lines TDCs.

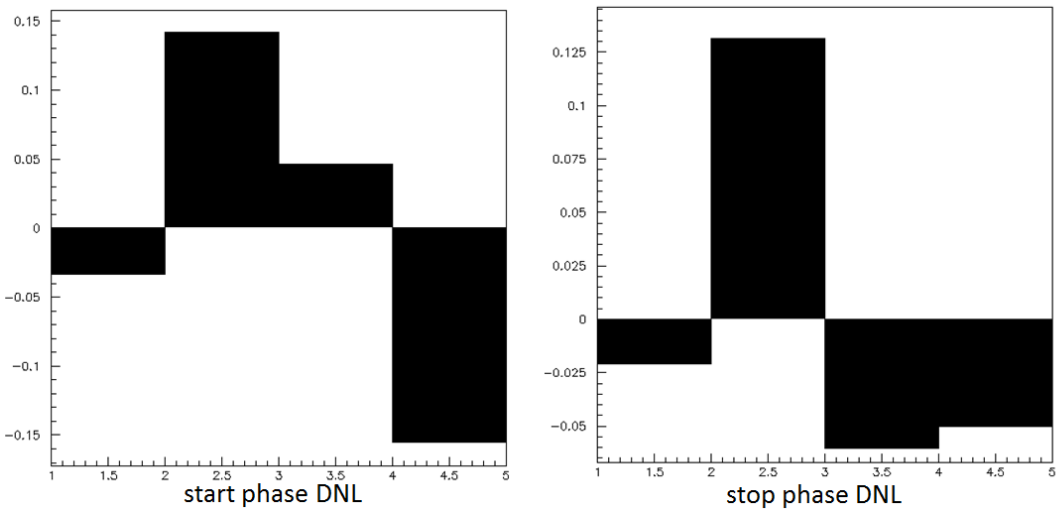


Figure 5.12: Phase occupancy distribution's differential non linearity for the TDC flash architecture. Left: Start phase DNL. Right: Stop phase DNL.

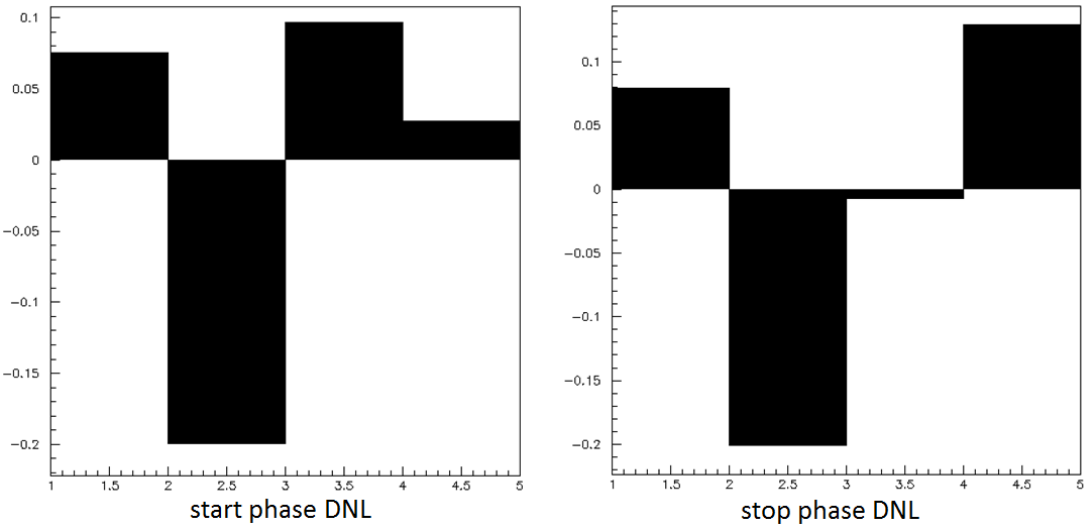


Figure 5.13: Phase occupancy distribution's differential non linearity for the TDC Vernier architecture. Left: Start phase DNL. Right: Stop phase DNL.

Figure 5.14 and 5.15 show the INL for the phase occupancy distribution of the start and stop signals for the flash and Vernier delay lines TDCs.

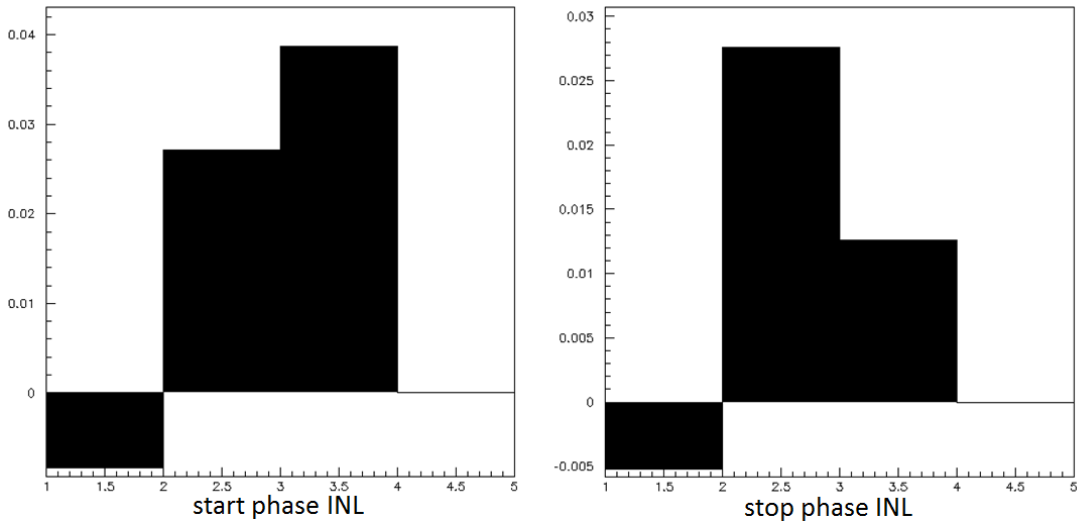


Figure 5.14: Phase occupancy distribution's integral non linearity for the TDC flash architecture. Left: Start phase INL. Right: Stop phase INL.

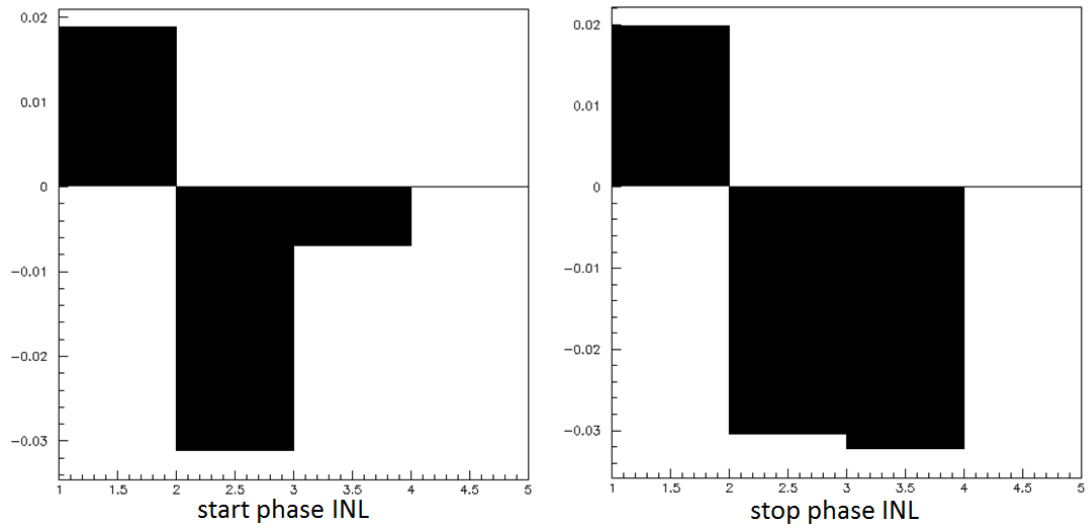


Figure 5.15: Phase occupancy distribution's integral non linearity for the TDC Vernier architecture. Left: Start phase INL. Right: Stop phase INL.

These measurements can be used to execute a preliminary calibration of the coarse TDC. The DNL and INL plots verify that the width of the phase measured by the second stage of the TDCs are not exactly a quarter of the clock period but slightly different from it; these deviations are lower than 20%.

5.5.2 Carry chain delay line calibration

I executed tests of the carry chain delay lines. These lines are the third stage of the TDC architecture. Figure 5.16 shows a plot of the hit counts as function of the channel number for the four start delay lines. I did 160000 measurements. The clock frequency is 550MHz. The operating temperature was of about 30 °C. The start signal delay lines numbered from 1 to 4 are sampled between the 0° and 90°, 90° and 180°, 180° and 270° and 270° and 360° respectively.

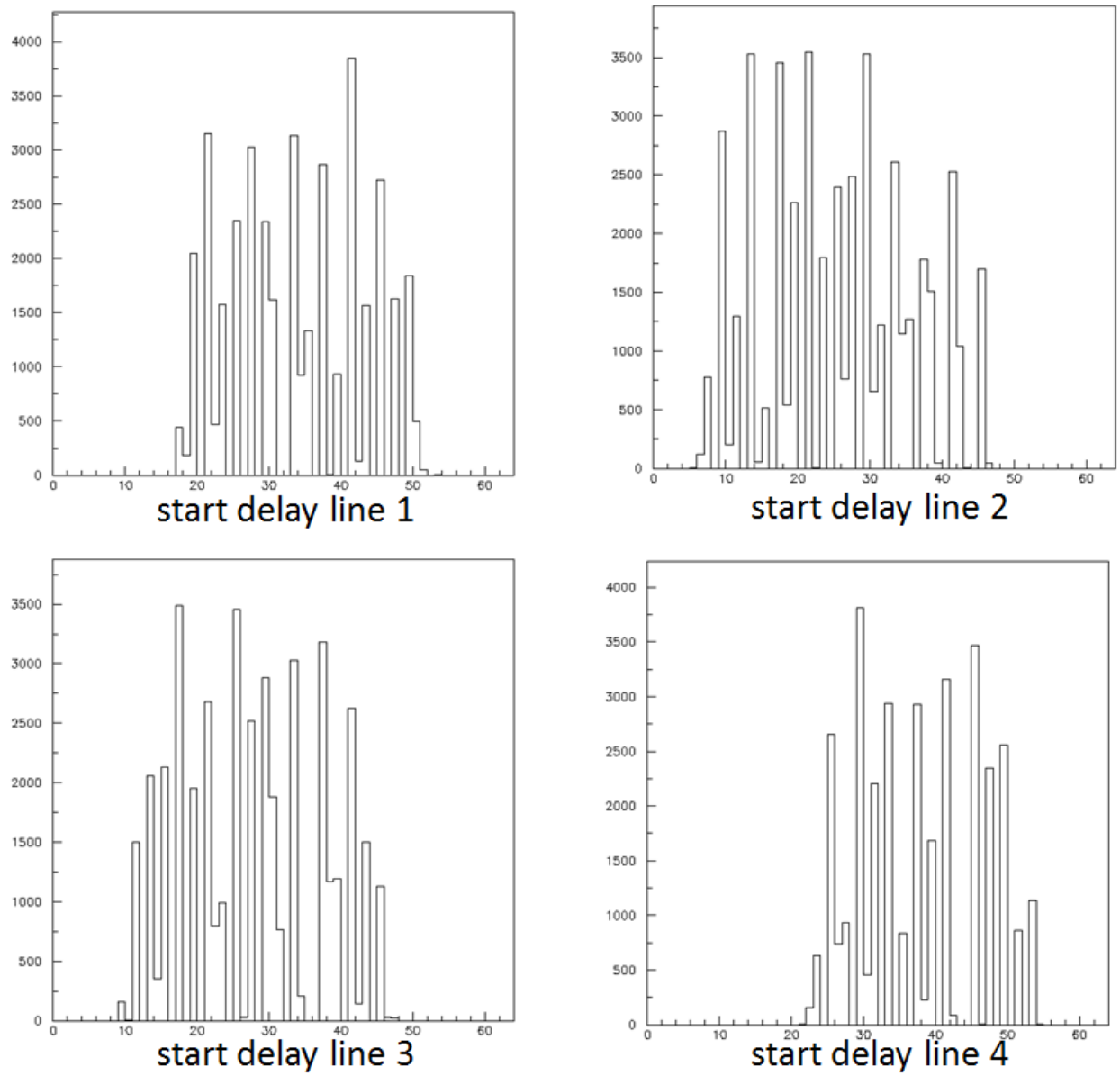


Figure 5.16: Hit count as function of the channel number for the start carry chain delay lines.

The time interval measuring range for each delay line can be determined from the start phase occupancy of the second stage output, shown in figure 5.10 (left), by means of the relation:

$MR_i = T * \frac{N_i}{N}$, where MR_i is the measuring range of the i-th delay line, T is the clock period, N is the total number of measurements, N_i is the number of measurements inside the i-th phase.

The measured time interval range for the first delay line is between 0 and about 437 ps (1818 ps * $\frac{38500}{160000}$), for the second one is between 0 and about 517 ps (1818 ps * $\frac{45500}{160000}$), for third one is between 0 and about 477 ps (1818 ps * $\frac{42000}{160000}$), for the last one is between 0 and about 386 ps (1818 ps * $\frac{34000}{160000}$). The number of active cells is 37, 41, 39 and 34 for the first, second, third and fourth delay line respectively. Therefore the mean propagation time of every buffer of the four lines is between 10 and 11 ps.

Figure 5.17 shows a plot of the hit counts as function of the channel number for the four stop delay lines. The same considerations of the start delay lines may be referred to the stop delay lines.

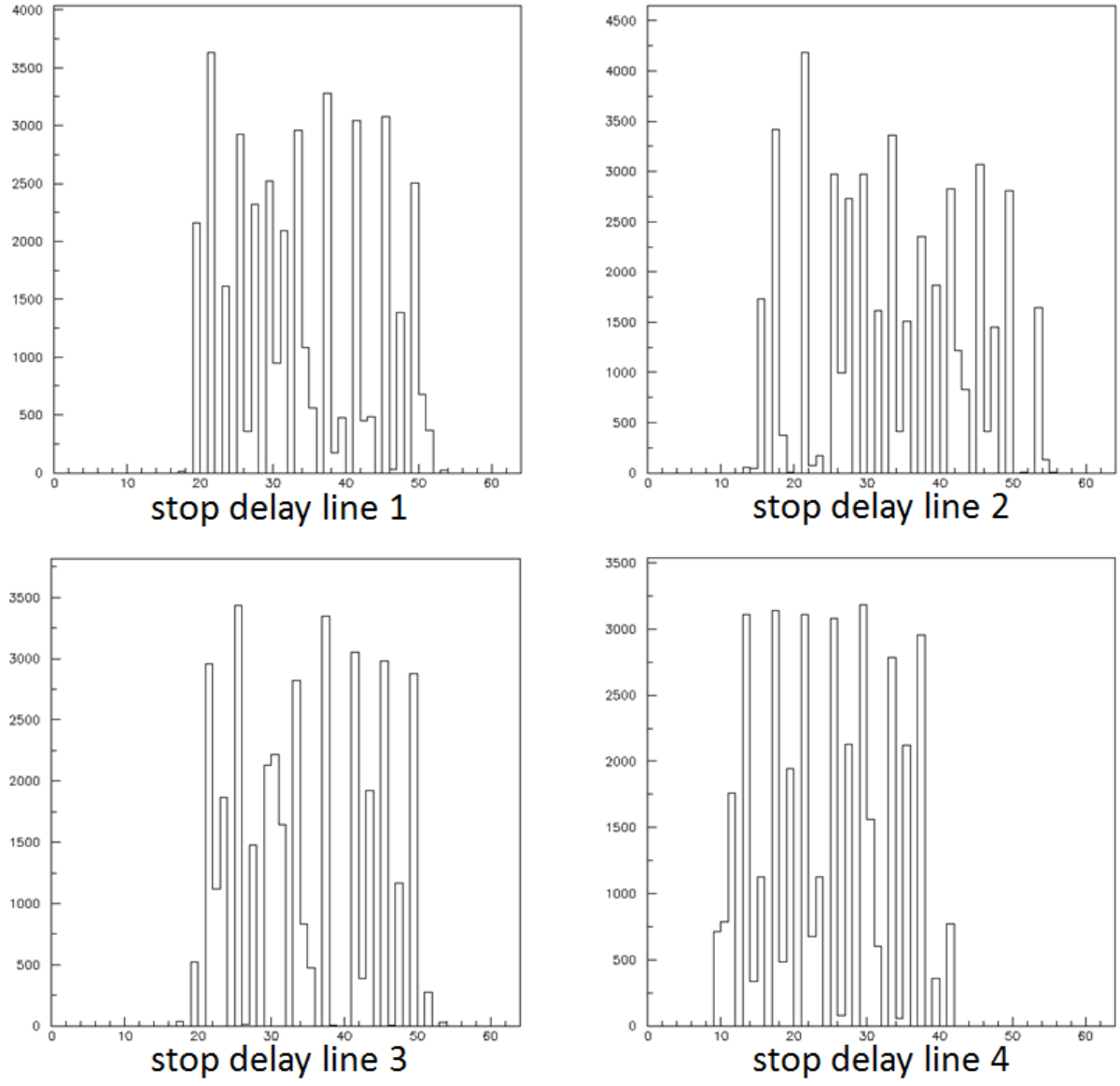


Figure 5.17: Hit count as function of the channel number for the stop carry chain delay lines.

The plots show some non-uniformity due to the structure of the device. In fact there are some missing fields in the plot, they are due to the internal structure of the slice. The propagation time inside every slice is really short. The slice is divided in two substructure made of a couple of flip-flop. In fact the propagation time of the first and the third multiplexer inside the slice are so small that the first couple of flip-flop switches always together, while the second couple of flip-flop switches often together. The hit count as function of the channel number for the start and stop delay lines is used to execute a further calibration; in fact every bin of the delay lines distribution means a time step, bin most populated means longer time step. The value of each time step TS_i is given by the maximum time interval measured by each delay line (delay length, DL) multiplied by the number of counts inside that bin normalized to the total hit counts for that delay line: $TS_i = DL * \frac{\text{bin i counts}}{total\ hit\ counts}$. Figure 5.18 shows the differential non linearity as function of the channel number for the four start delay lines.

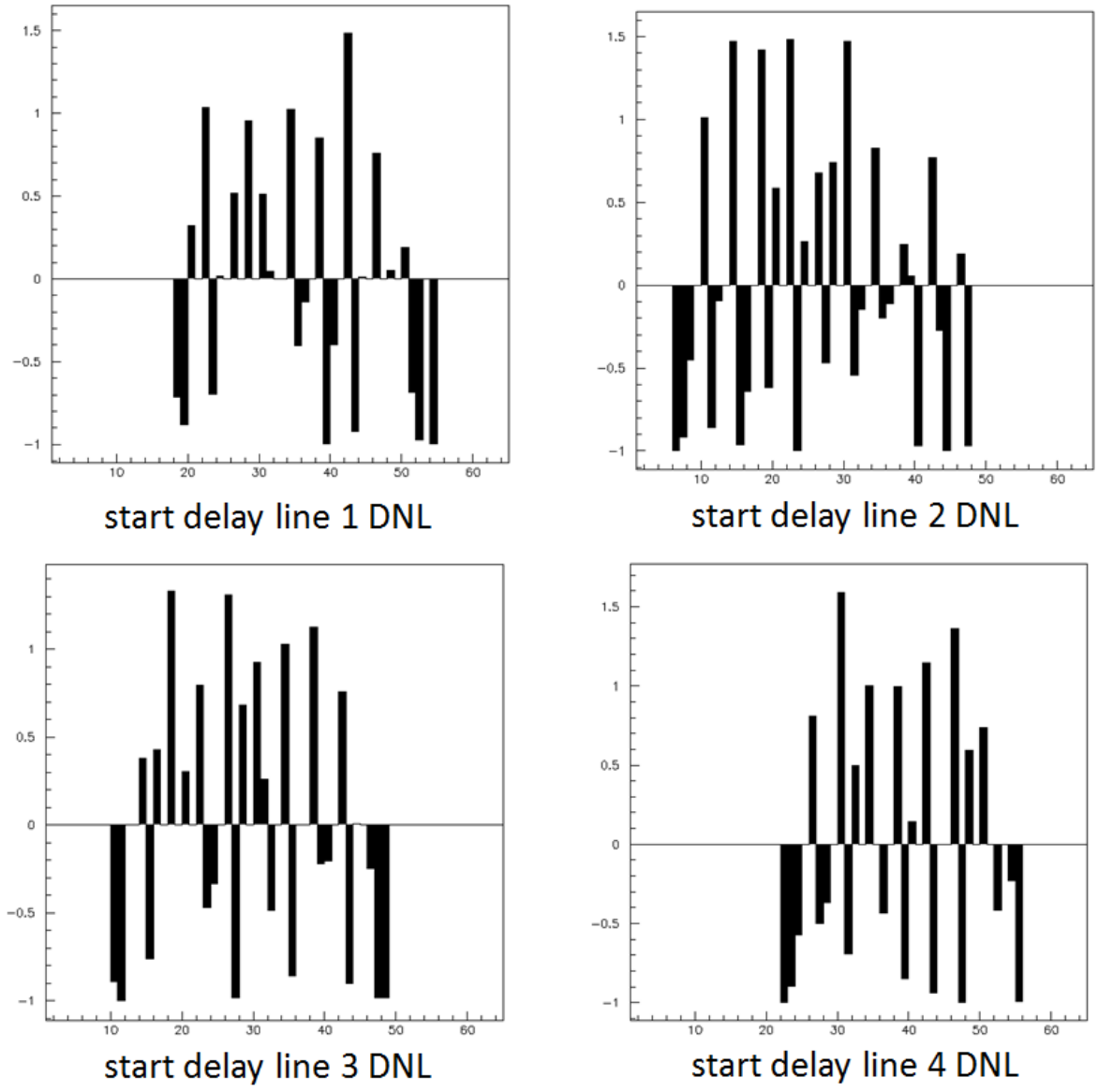


Figure 5.18: Differential non linearity as function of the channel number for the start carry chain delay lines.

Figure 5.19 shows the differential non linearity as function of the channel number for the four stop delay lines.

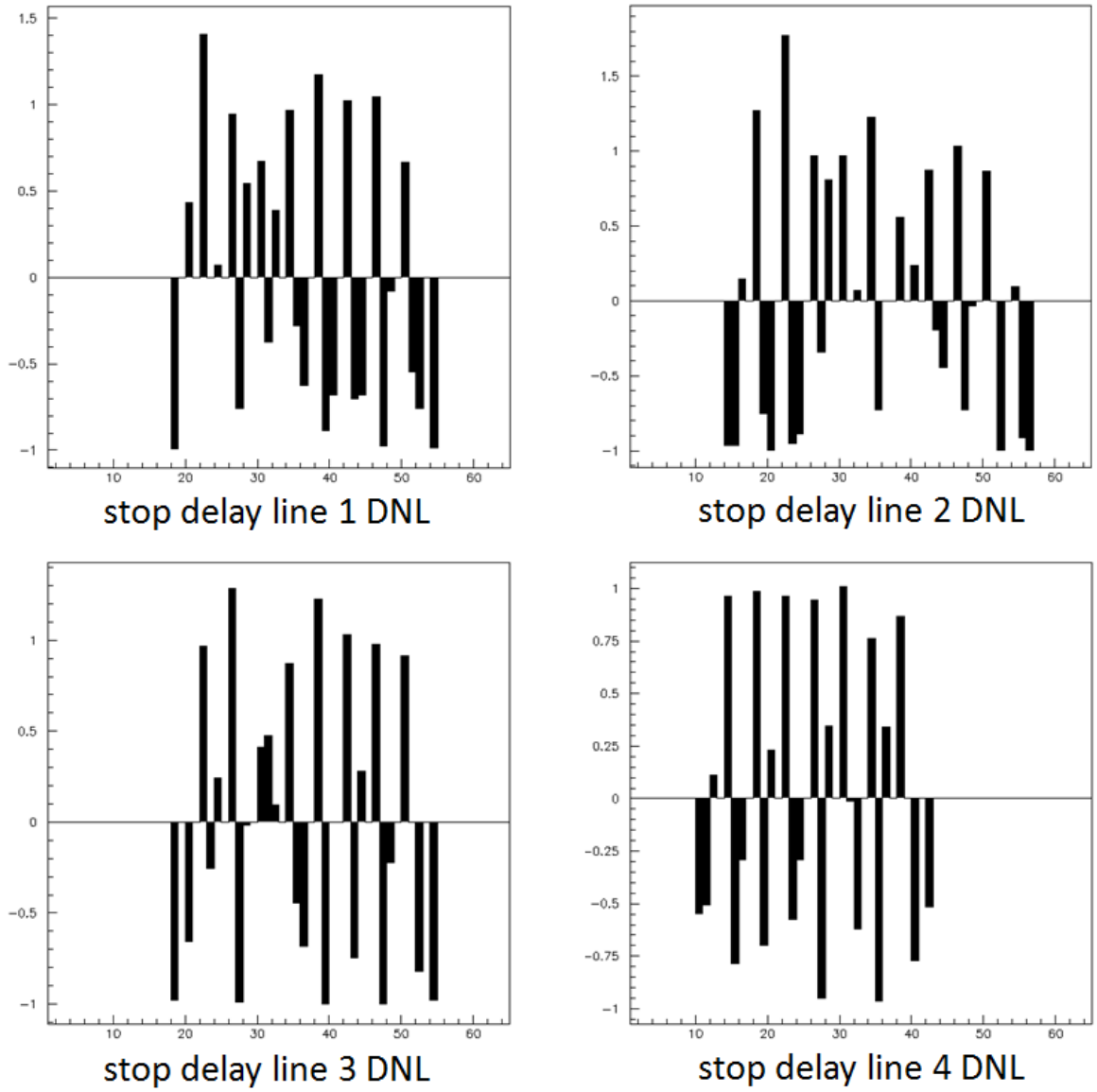


Figure 5.19: Differential non linearity as function of the channel number for the stop carry chain delay lines.

Figure 5.20 shows the integral non linearity as function of the channel number for the four start and stop delay lines.

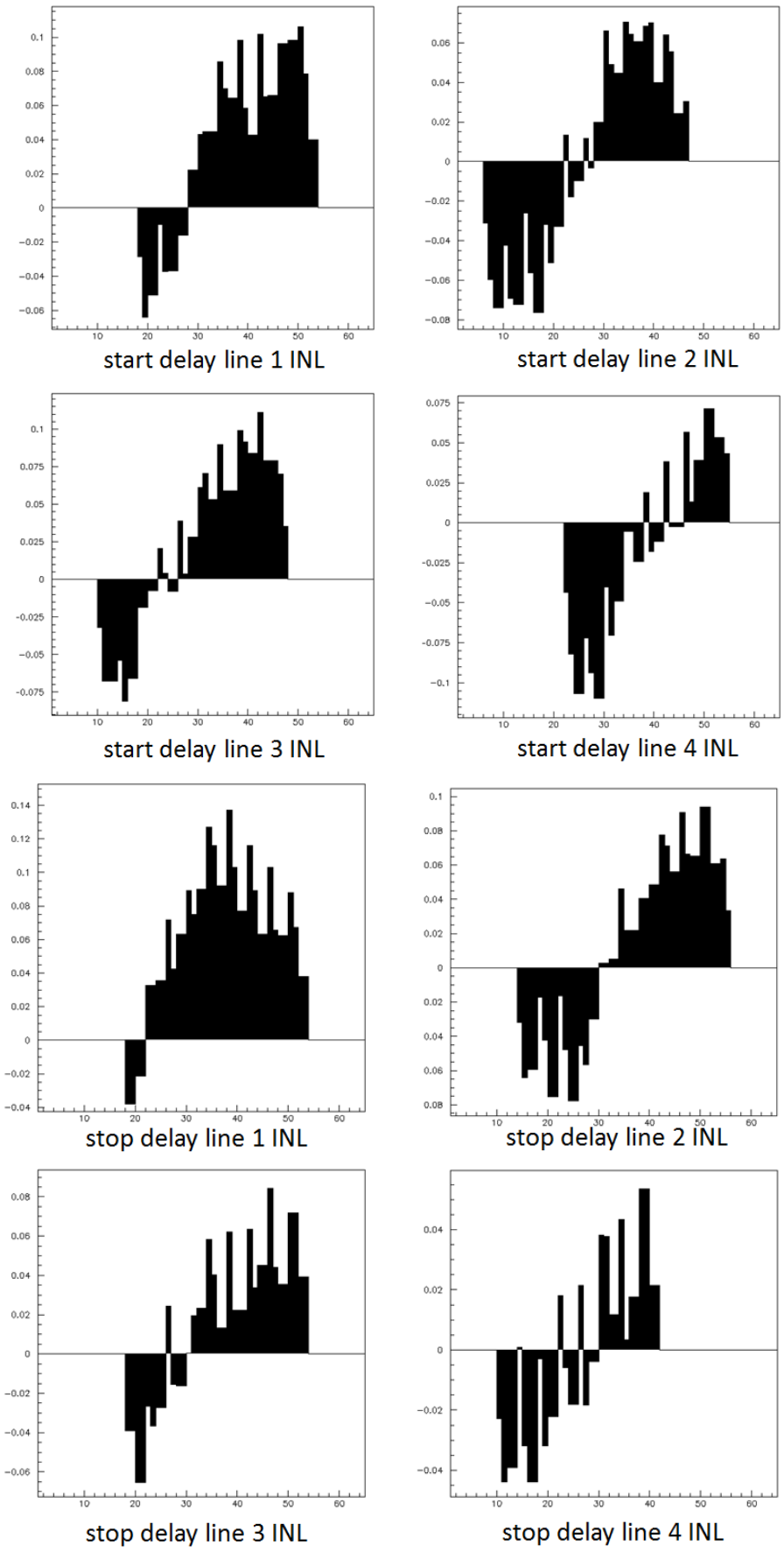


Figure 5.20: Integral non linearity as function of the channel number for the four start and the stop carry chain delay lines.

5.5.3 Carry chain delay line time measurements

The Carry chain delay line TDC has been calibrated and then, several time measurements were made. The operating temperature oscillated in a range of 1 degree around 30°C during the data taking. Figure 5.21 shows a test result of the TDC output as a function of the input time interval to be measured. Each point of the plot is made by the average of 160000 measurements. The TDC is linear up to 20 us and the resolution is between 16 ps and 35 ps in every measured point in that time interval. Figure 5.22 shows the resolution of the system, constituted by the pulsing system and the TDC, as function of the generated time interval. The resolution is calculated as the RMS value of 160000 measurements for every single point of the plot.

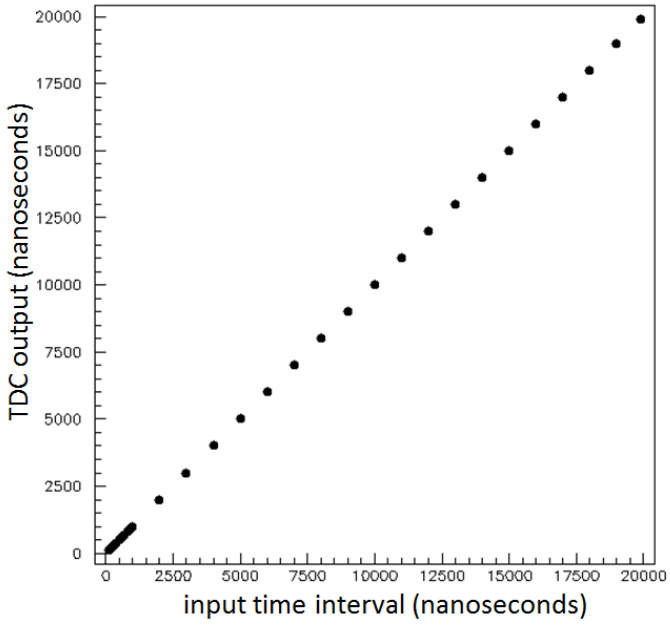


Figure 5.21: Carry chain delay line TDC output as function of the input time interval.

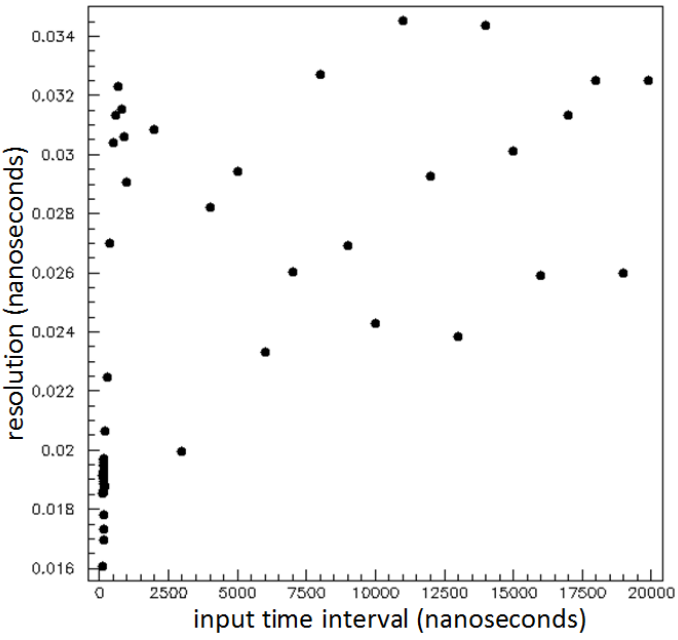


Figure 5.22: Carry chain delay line TDC resolution as a function of the input time interval.

5.5.4 Carry chain delay line time measurements vs. operating temperature

The Carry chain delay line TDC has been tested under different operating temperature ranging from 25°C to 75°C. Figure 5.23 (left) shows a plot of the operating temperature as function of the elapsed time. Figure 5.23 (right) shows a plot of the TDC resolution as function of the operating temperature for a 100 ns time interval measurements; 160000 measurements for each point of the plot were made. The resolution is between 17 ps and 26 ps; it increases by about 0.18 ps/°C.

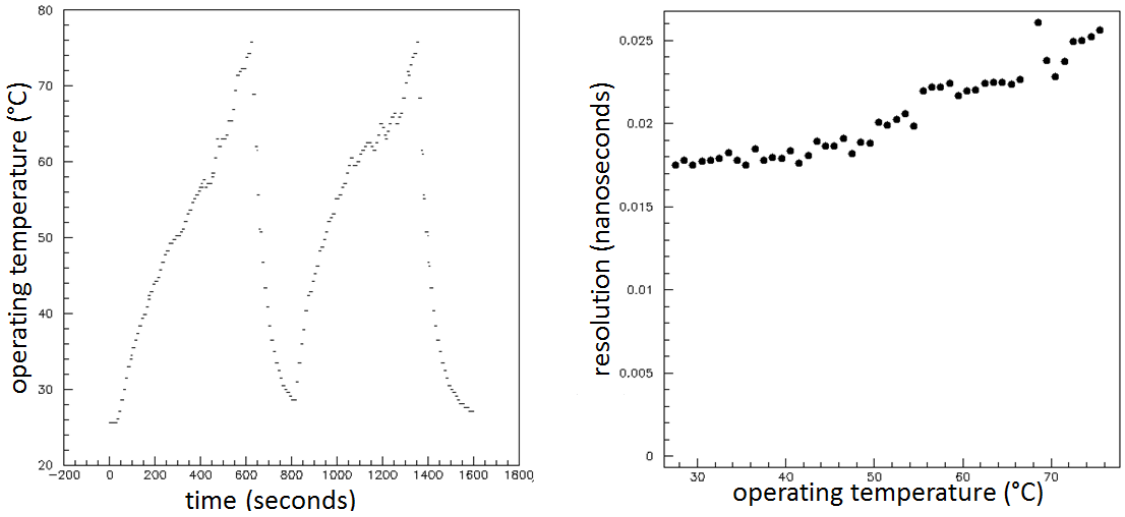


Figure 5.23: Thermal cycles. Left: Operating temperature as function of the elapsed time. Right: Carry chain delay line TDC resolution as a function of the operating temperature.

5.5.5 Vernier delay line calibration

I executed tests of the Vernier delay lines; they are the third stage of the TDC architecture. Figure 5.24 shows a plot of the hit counts as function of the channel number for the four start and stop Vernier delay lines. I made 160000 measurements. The clock frequency is 550MHz. The operating temperature was of about 30 °C. I sampled the start signal along the delay line 1 between the 0° and 90° phases of the clock signal, the delay line 2 between the 90° and 180° phases of the clock signal, the delay line 3 between the 180° and 270° phases of the clock signal, the delay line 4 between the 270° and 360° phases of the clock signal. Some non-uniformities are due to the internal layout structure of the device. As in the flash architecture, the hit count as function of the channel number for the start and stop delay lines is used to execute a further calibration; the value of each time step TS_i is calculated in the same way. The mean time step of the lines is between 14 and 16 ps.

Figure 5.25 shows the differential non linearity as function of the channel number for the four start and stop Vernier delay lines.

Figure 5.26 shows the integral non linearity as function of the channel number for the four start and stop Vernier delay lines.

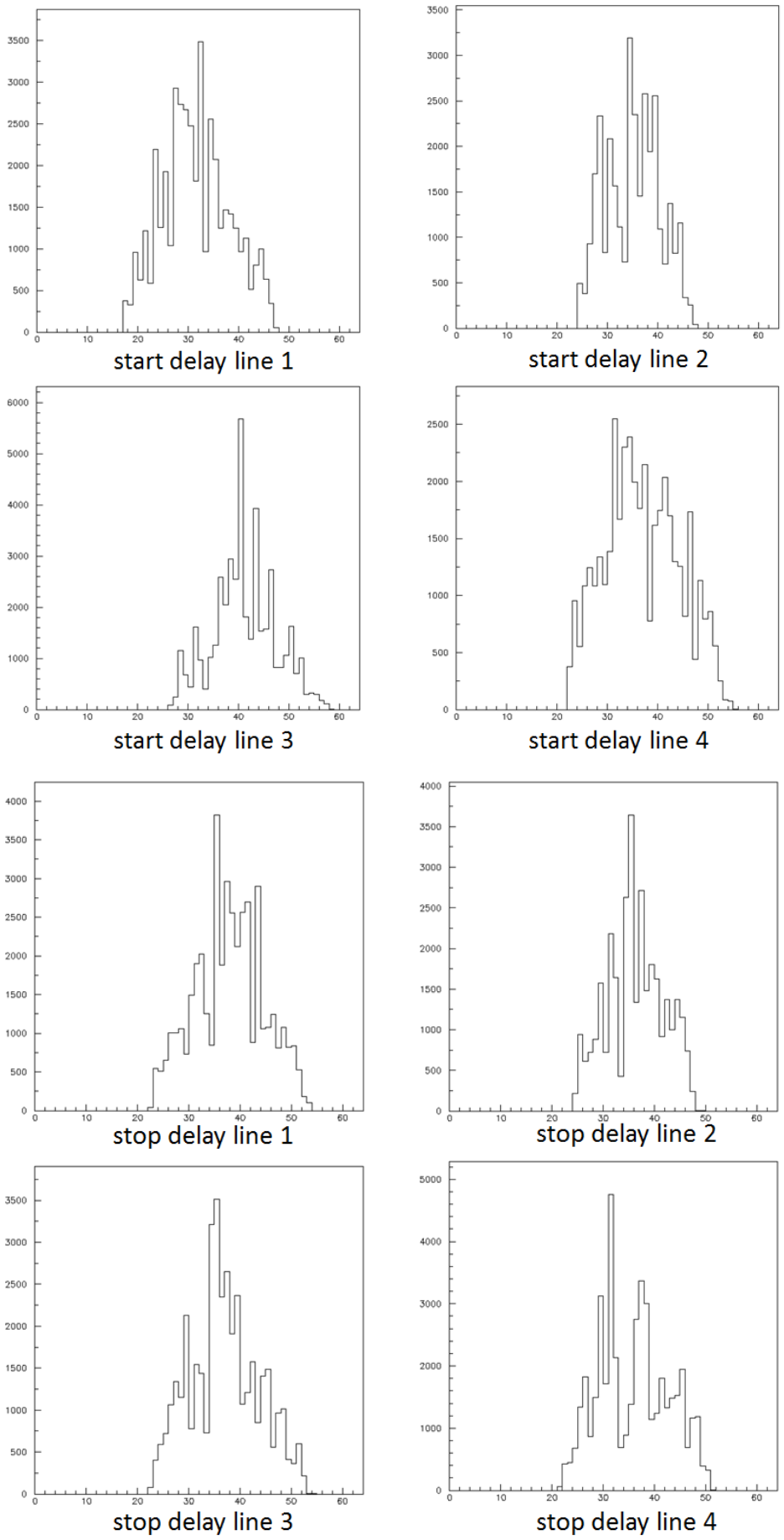


Figure 5.24: Hit count as function of the channel number for the start and stop Vernier delay lines.

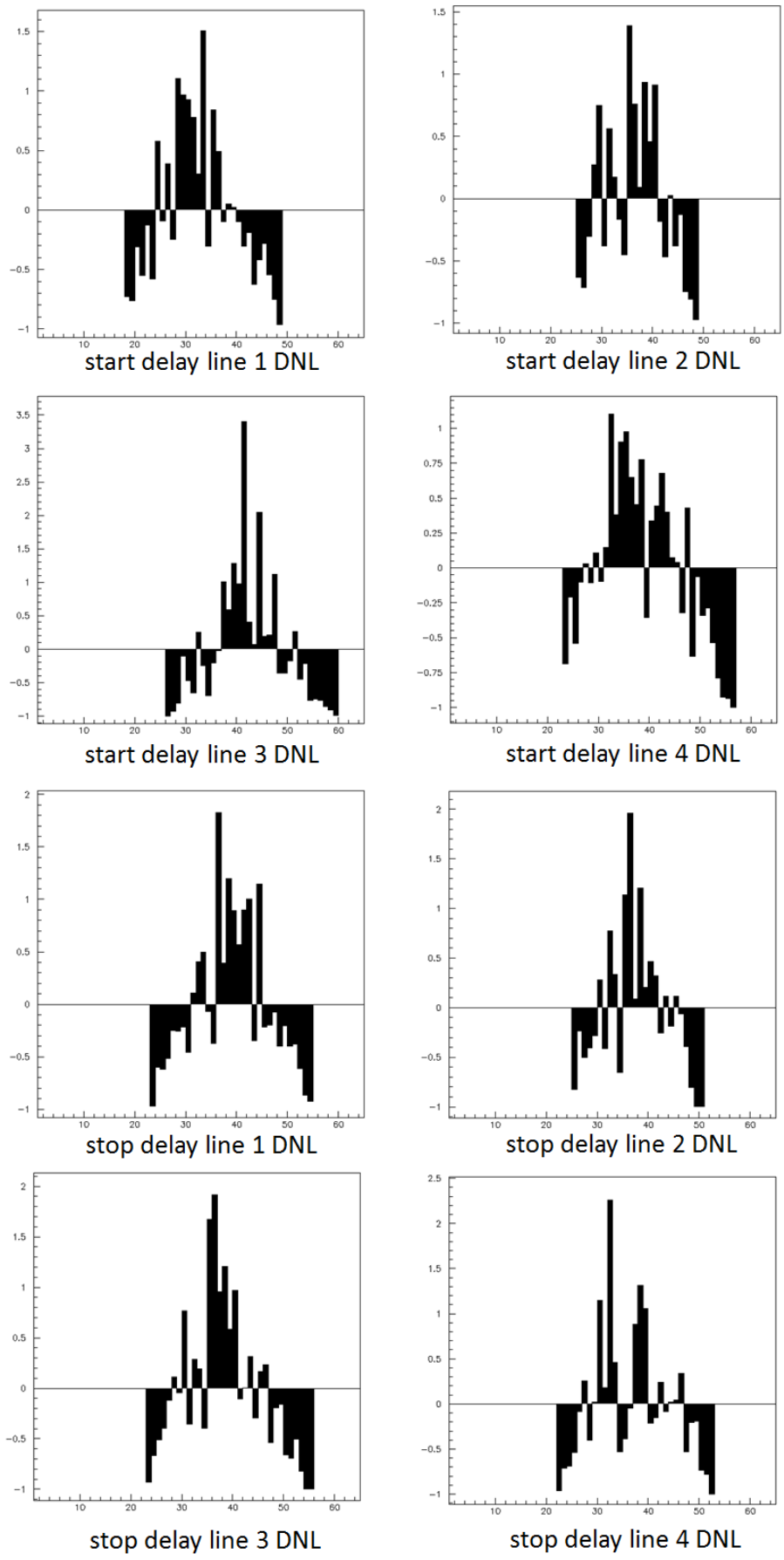


Figure 5.25: Differential non linearity as function of the channel number for the start and stop Vernier delay lines.

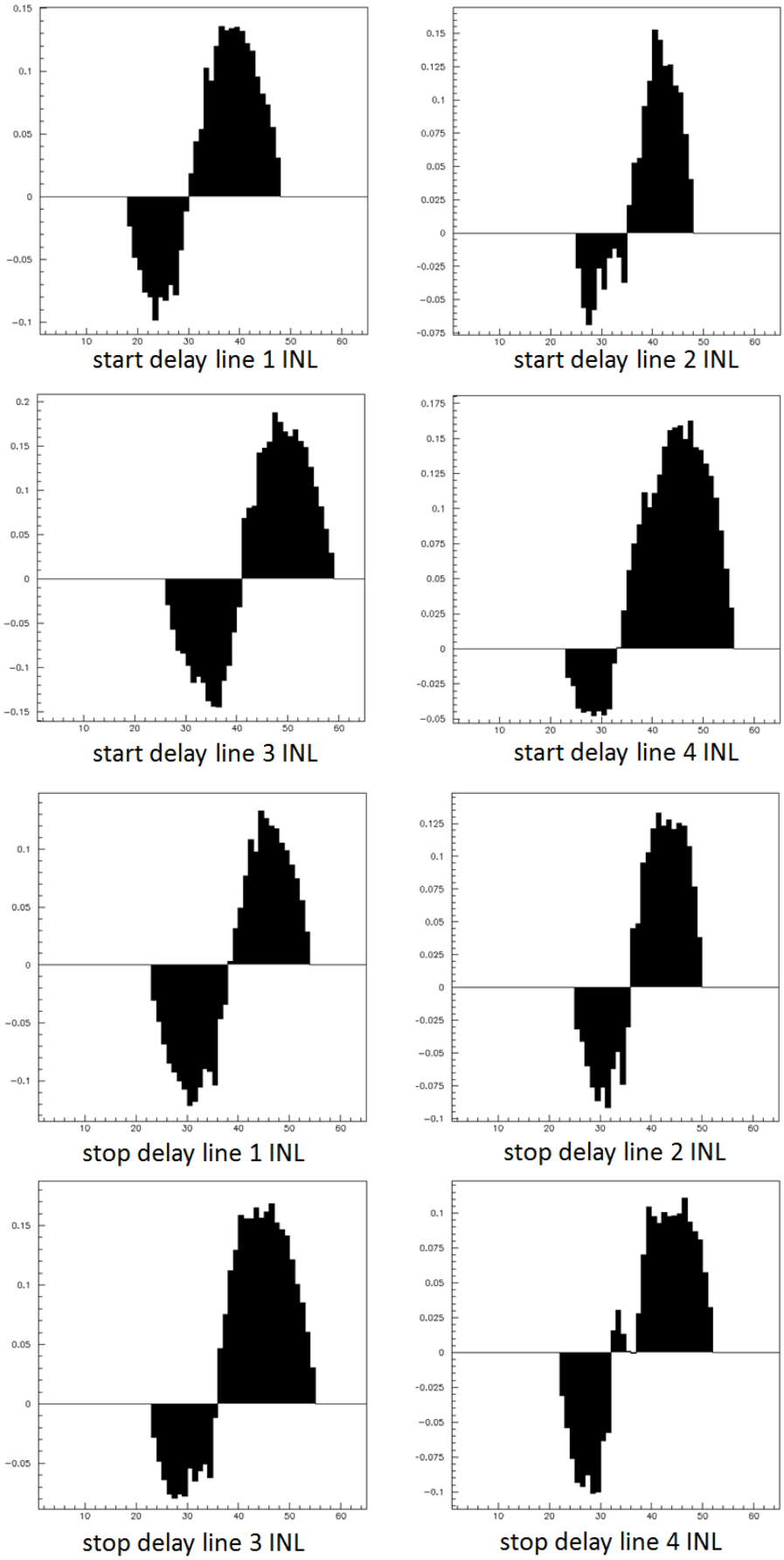


Figure 5.26: Integral non linearity as function of the channel number for the start and stop Vernier delay lines.

5.5.6 Vernier delay line time measurements

The Vernier delay line TDC has been calibrated and then, several time measurements were made. The operating temperature oscillated in a range of 1 degree around 30°C during the data taking. Figure 5.27 shows a test result of the TDC output as a function of the input time interval to be measured. Each point of the plot is made by the average of 160000 measurements. The TDC is linear up to 20 us and I have measured a resolution between 46 ps and 142 ps in every measured point in that time interval. Figure 5.28 shows the resolution of the system, constituted by the pulsing system and the TDC, as function of the generated time interval. The resolution is calculated as the RMS value of 160000 measurements for every single point of the plot.

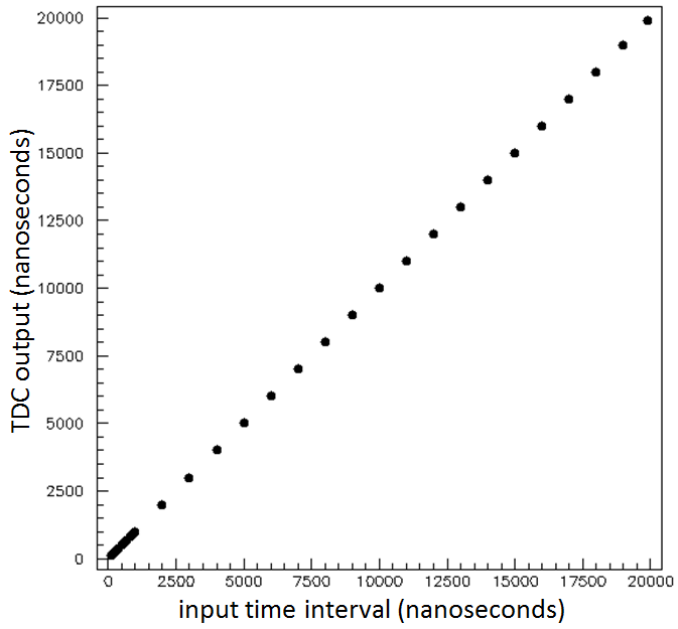


Figure 5.27: Vernier delay line TDC output as function of the input time interval.

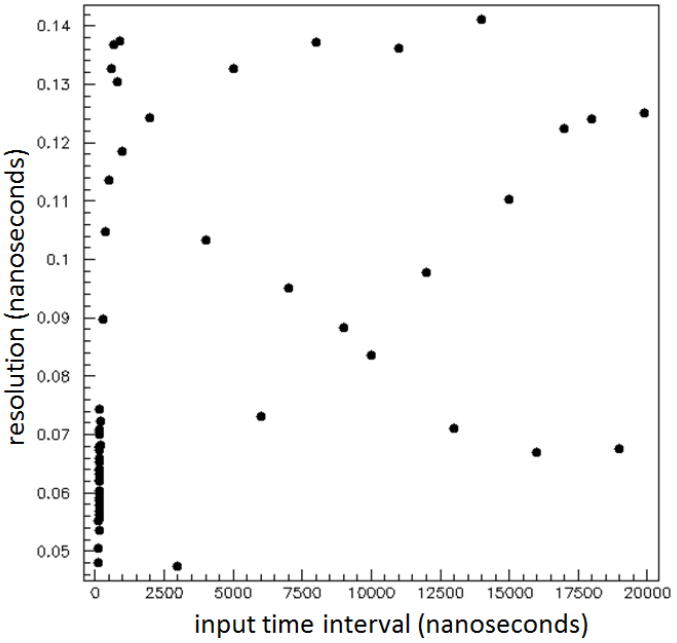


Figure 5.28: Vernier delay line TDC resolution as a function of the input time interval.

5.5.7 Vernier delay line time measurements vs. operating temperature

The Vernier delay line TDC has been tested under different operating temperature ranging from 25°C to 75°C. Figure 5.29 (left) shows a plot of the operating temperature as function of the elapsed time. Figure 5.29 (right) shows a plot of the TDC resolution as function of the operating temperature for a 100 ns time interval measurements; 160000 measurements for each point of the plot were made. The resolution is between 46 ps and 56 ps.

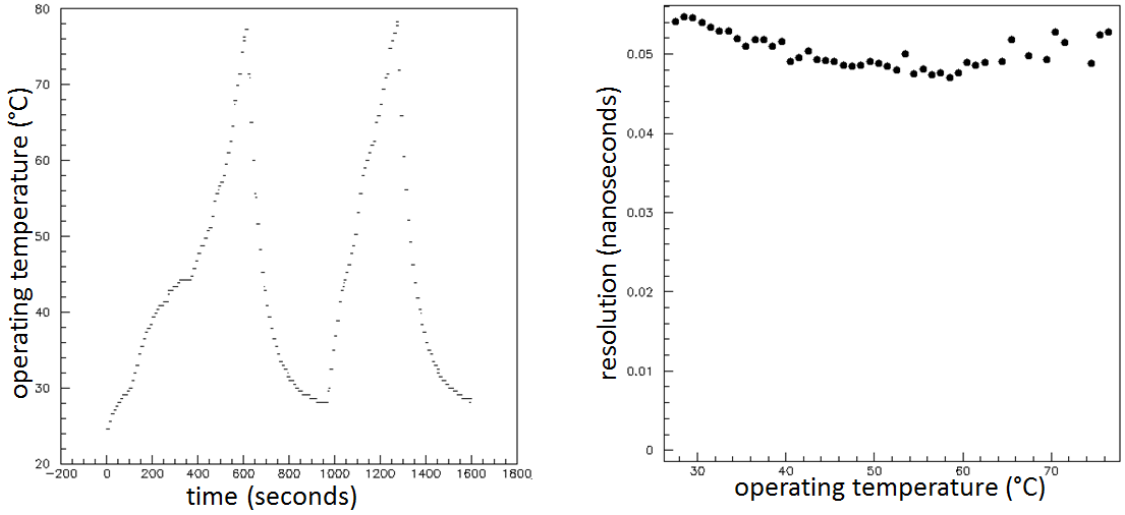


Figure 5.29: Thermal cycles. Left: Operating temperature as function of the elapsed time. Right: Vernier delay line TDC resolution as a function of the operating temperature.

5.5.8 Conclusions

Semiconductor devices are becoming faster and faster. This allows to have high resolution digital counter and short delay elements. Therefore, it is possible to develop a low cost and high resolution TDC exploiting FPGAs based techniques. By using SRAM-based FPGAs, the user benefits from the in system programming (ISP) and reconfiguration features increasing the flexibility and reliability of the measuring system. The architectures implemented show very good performance in terms of time resolution; they are linear up to 20 us of range of measurements. I have measured in every points in that time interval a resolution between 16 ps and 35 ps for the TDC flash architecture and a resolution between 46 ps and 142 ps for the TDC Vernier delay line architecture.

The dead time is the shortest time interval between the end of a measurement and the start of the next one. The dead time is 12.7 ns (for a 550 MHz clock) for the TDC flash architecture and 32.7 ns (for a 550 MHz clock) for the TDC Vernier architecture. The TDC can be used also in multi hit mode; i.e. it can be used in multi stop mode, in that case the number of stop events is limited by the

FIFO used to register the time intervals binary output. The minimum time distance between two subsequent stop events is given by the dead time of the TDC.

The TDCs calibration constants (measured at 30°C) could be used in a range of temperatures from 25°C to 75°C with slightly worsening the time resolution; so it's not necessary to recalculate them for different temperatures, but eventually in order to further improve the time resolution an embedded microprocessor could be used to achieve that task. The carry chain TDC time resolution increases of about 0.18 ps/°C. In fact for a 100 ns time interval measurement; it is between 17 ps (at 25°C) and 26 ps (at 75°C) for a 50°C temperature shift. The Vernier delay line TDC time resolution doesn't change for a 50°C temperature shift. In fact for a 100 ns time interval measurement; it is about 50 ps for the entire 50°C temperature range.

The flash TDC architecture seems to be the best one; 16 channels could be implemented in the FPGA used for these tests. Furthermore the number of channels could be greater than 16, in the case the TDC architecture uses only the first and second stages, then without interpolating inside a quarter of the clock period. The resolution should be given by $\frac{454\text{ ps}}{\sqrt{12}}$ = 131 ps (for a 550 MHz clock). The dead time could be lower than 10 ns and the number of channels could grow. In this case, the architecture is much simpler, therefore less FPGA resources are used. It implies a lower number of place and route constraints and it is less time consuming.

The number of channels could reach 64 or higher, but it should not be limited by the occupancy of the device but probably by signal integrity problems; such as crosstalk between channels.

Chapter 6

Conclusions

In this thesis work, I studied the problem of building a high resolution Time to Digital Converter implemented in a Field Programmable Gate Array. For many years the main methods used to achieve the hundreds of pico-seconds resolution have been based on time-stretching, Vernier and tapped delay lines. In general, the digital methods are preferred because the analogue methods are difficult to implement in the integrated circuit technology, more sensitive to the ambient temperature and more susceptible to external disturbances and have a longer conversion time.

Different configurations of tapped delay lines are widely used to measure nanosecond time intervals both in ASIC and FPGA devices. However, the design process of an ASIC device can be expensive, especially if produced in small quantities, while FPGAs reduce the development cost and offer high design flexibility. In fact, by using SRAM-based FPGAs, the user benefits from in-system-programming (ISP) and reconfiguration features increasing reliability of the measuring system.

The newest available FPGAs allow to achieve high speed digital design. This means high resolution digital counter and then a reduced number of delay elements of the line used for the time interpolation within the system clock cycle. Furthermore they allow to phase shift the clock signal in order to perform a first level phase interpolation. So the delay lines are used to interpolate the time measurements within a single phase of the clock cycle. This strategy further reduces the length of the delay lines and then the non linearity introduced by the lines.

I designed two types of TDC architectures in the Xilinx Virtex-5 FPGA. I used the XCVLX50 with -3 speed grade in order to improve the performance for high-speed design. Both approaches use the classic Nutt method based on the two stage interpolation. The first architecture consists of tapped delay lines, while the second one uses Vernier delay lines.

Carry chain delay line TDC

The carry chain delay line TDC is based on a flash architecture, so besides being virtually dead time free, it is multi-hit. This architecture shows very good performance in terms of time resolution (between 16 ps and 35 ps up to 20 μs time interval). The dead time is 12.7 ns (for a 550 MHz clock).

The TDCs calibration constants (measured at 30°C) could be used in a range of temperatures from 25°C to 75°C slightly worsening the time resolution. The time resolution increases of about 0.18 ps/°C. In fact for a 100 ns time interval measurement; it is between 17 ps (at 25°C) and 26 ps (at 75°C) for a 50°C temperature shift.

Vernier delay line TDC

The Vernier delay line TDC shows a slightly worse performance in terms of time resolution then the flash architecture.

I have measured a resolution between 46 ps and 142 ps up to 20 μs time interval. The dead time is 32.7 ns (for a 550 MHz clock). The time resolution doesn't change for a 50°C temperature shift (range of temperatures from 25°C to 75°C). In fact for a 100 ns time interval measurement; it is about 50 ps for the entire 50°C temperature range.

Long range time interval measurements

The long range time measurements were made for time intervals extending until seconds.

These tests show that the commercial quartz oscillators can still be used for measurements of short time intervals (100/200 ns) and measurements that do not require very high precision; while for time measurements requiring high precision, a high stability oscillator should be used. The high stability oscillator used in these tests has a temperature stability up to 5 ppb over a temperature range from -40°C to +85°C. It maintains reasonably good stability and precision for the entire range of measurements.

Conclusions and future developments

The flash TDC architecture seems to be the best one. Up to 16 channels could be implemented in the FPGA used for these tests. The resolution values obtained are well fitting the needs of the time measurements of the KLOE experiment. In fact, in the KLOE experiment, the dynamic range is

defined by the kinematics of kaon decays (the K_L meson lifetime is about 50 ns); so the range of measurement needed is about 200-300 ns. In this range the carry chain delay line TDC shows a very good resolution of about 20 ps. Furthermore, the range of measurement of this kind of TDC is not limited to that value, but can easily extend until 20 μs with a time resolution below 35 ps.

Moreover such a TDC is virtually dead time free; it implies its use in high trigger rate environment like Super B Factories where the estimated trigger rate is about 150 KHz at a luminosity of 10^{36} cm^{-2} s^{-1}.

If such high resolution time measurements are not required, the TDC architecture can be simplified by removing the delay lines stage.

In this case, the architecture is much simpler and therefore less FPGA resources are used. It implies a lower number of place and route constraints and it is less time consuming.

The number of channels could be 64 housed in the FPGA used for this tests or higher, not limited by the occupancy of the device but probably limited by signal integrity problems; such as crosstalk between channels.

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